FPGA IMPLEMENTATION OF SELECTIVE HARMONIC ELIMINATION FOR CASCADED MULTILEVEL INVERTER WITH ADJUSTABLE DC SOURCES USING ARTIFICIAL BEE COLONY ALGORITHM

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Abstract---This paper presents a methodology for arriving at the switching angles for a step modulated eleven level inverter comprising of a set of five cascaded H Bridge (CHB) inverters operated with five adjustable DC voltage sources using Artificial Bee Colony (ABC) Algorithm. More number of bridges can eliminate more number of harmonics while the equation set to be solved also becomes larger and larger and the computerized but traditional algebraic procedures also become helpless. However with heuristic search algorithms it is possible to estimate the solutions within the limits of allowable tolerances even if the number of equations is large. Of the many available heuristic algorithms the ABC Algorithm is a competitive candidate that can be realized in hardware in real time as well. Both MATLAB based simulation and an experimental Hardware using Field Programmable Gate Array (FPGA) Spartan 6A DSP were set up and the results are promising. The results are compared with PSO and it is proved that the proposed method offers reduced THD with less computation period.

Keywords: Cascaded Multilevel Inverter, Artificial Bee Colony Algorithm, Selective Harmonic Elimination, FPGA

1. INTRODUCTION

The advantages of the cascaded Multilevel Inverters (MLI) have made it possible that they find places in many industrial applications in the recent past. The cascaded MLIs can be used to integrate isolated DC voltage sources with equal or unequal DC voltage levels to provide an AC voltage output that is better in power quality compared to the conventional two level inverters. With lower rated components, high voltage and high power capabilities can be achieved with the MLIs [1]. Non-conventional energy sources like the Photo Voltaic Sources, the wind power conversion system and generation schemes based on Fuel cells can all be used in the synthesis of AC voltages close to a sinusoidal wave. Flexible AC transmission systems and the HVDC systems also offer a good place for the MLIs [2]. Another area of application of the MLIs encompasses is the electrical drives systems. Electrical motors like the three phase induction motors which account for nearly 90% of consumption of the generated power worldwide. With electric drives using induction motors which exhibit low pass characteristics, the Selective Harmonic Elimination (SHE) is more appropriate since the lower order harmonics are eliminated in the source itself and the higher order harmonics can be filtered by the load itself [3]. With MLIs, thanks to the modern modulation methods, the much reduced Common-Mode (CM) voltage reduces the stress in the motor bearings. Lower switching frequency associated with SHE PWM directly returns with improved efficiency with the reduction of switching losses.

MLIs, subject to the type of DC voltage sources available, are classified as cascaded H bridge type and non H bridge type. Wherever there are isolated DC sources, cascaded H bridge MLI [4, 5] will be the better choice, and if what is available is a single DC source then the natural option is the diode clamped MLI [6] or the flying capacitor type of inverter [7]. Among them the cascaded H-bridge [CHB]

topology is found to be suitable for distributed energy applications. The problem of instability arises in converters due to the harmonics which are integral multiples of the fundamental frequency. The harmonics present in the output of a dc to ac inverter can be eliminated either by using filter circuit or by employing pulse width modulation (PWM) technique. The problems of larger size filter and associated cost can be swept away with PWM techniques depending on the type of application.

In [8] the authors have discussed about the techniques used for switching the MLI with low switching frequency scheme. The Selective Harmonic Elimination PWM is one among the various low frequency switching strategies. In SHE PWM technique it is necessary to solve a set of trigonometric transcendental equations. The predominant method of solving the transcendental equations describing the SHE PWM strategy is by means of iterative techniques including the Newton Raphson technique [9]. The function to be solved should necessarily be differentiable and that proper initial guess is required. The Newton Raphson method gives the solution that is next nearest as dictated by the initial guess. Another analytical method is the theory of resultants and it is capable of finding all feasible solutions [10]. Considering the mathematical complexity, the theory of resultants is a difficult procedure especially when handling more number of levels and it is much more complicated when the operating DC voltage sources varying from time to time in real time. While the classical algebraic techniques become helpless, the heuristic algorithms can handle the situation without an initial guess and also they arrive at the globally acceptable solutions sets.

The estimation of switching angles by solving the SHE equations have been demonstrated by using other heuristic search algorithms typically like the Genetic Algorithm[11,12] Particle Swarm Optimization (PSO) [13,14], Bacterial Foraging Algorithm [15], Differential Evolution[16], Clonal Search Algorithm [17] and Bees Algorithm [19]. Also SHE using neural network was demonstrated in [18].

Bees algorithm [19] was implemented for 7 level MLI with equal dc sources [20]. But practically the availability of dc sources is not always equal. In this scenario the ABC Algorithm [21] comes out as a better candidate considering the facts that it is capable of locating the globally optimal solution set, being less mathematically complex, higher speed of convergence and it's suitability for implementation in real time digital processor units

The proposed methodology has been validated using Matlab Simulink based simulation environment. A suitable experimental hardware has also been fabricated using FPGA. For the digital control of Power Electronic converters, Microcontrollers and DSPs are used where the no. of PWM pulses generated are limited. Hence FPGA is a better solution for the implementation of PWM algorithms of high Power Converters. In [22], Variable Common mode injection PWM for three level inverter is implemented using FPGA .In this proposed work, FPGA is used for the implementation of SHE and the results validate the simulation results obtained.

Next to the introduction, a review of cascaded MLI topology is presented in section 2 followed by a discussion on Selective Harmonic Elimination in Section 3. Section 4 gives a detailed treatment on the ABC Algorithm. The details of the simulation and the hardware setup along with a discussion on the results are summarized in Section 5 followed by the conclusion.

II. POWER TOPOLOGY OF CASCADED H BRIDGE MLI

Among the three types of MLIs, the CHB MLI has the least number of power devices for a given number of levels. It reaches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology. One feature which sets the cascaded H-bridge apart from other MLIs is the capability of utilizing different dc voltages on the individual Full bridge Inverter cells. The number of levels is proportional to the number of isolated Full Bridge Inverter [FBI] cells according to the expression $N = 2K + 1$, where K is the number of FBI per phase. In addition, the number of steps (Q) in the line voltage is $Q=2N-1$.The addition of a cell in each phase adds two more levels to the phase voltage and four more levels in the line voltage. An increase in the number of steps in the output voltage produces a reduction in harmonic distortion. The number of switch combinations is 2^{N-1}. For example, the number of switch combinations for five-level inverter is 16. Hence, the flexibility in voltage synthesizing for this topology is more than other types of MLI. An eleven-level CMI consists of five

individual cells; each containing its own FBI is shown in Figure 1. Each FBI uses a DC-link voltage to generate a modulated voltage at the output terminals. As the output side of the CHB inverter is connected in series, sources at the input side should be isolated from each other. Due to this property, H bridges are supplied from renewable energy sources like fuel cells, Photo Voltaic arrays etc. The output voltage of the i^{th} H-Bridge is given as $V_{Hi} = W_i \cdot V_{dc}$, where W_i is the switching function.

The value of W_i can be either 0 or 1 or 1. To obtain 0 either switches S_1 and S_2 or S_3 and S_4 are turned on simultaneously. To obtain +1, switches S_1 and S_4 are turned on, whereas −1can be obtained by turning on switches S_2 and S_3. The output Phase voltage waveform for 11 level cascaded MLI with five non equal dc sources ($S = 5$) is shown in Figure 2.

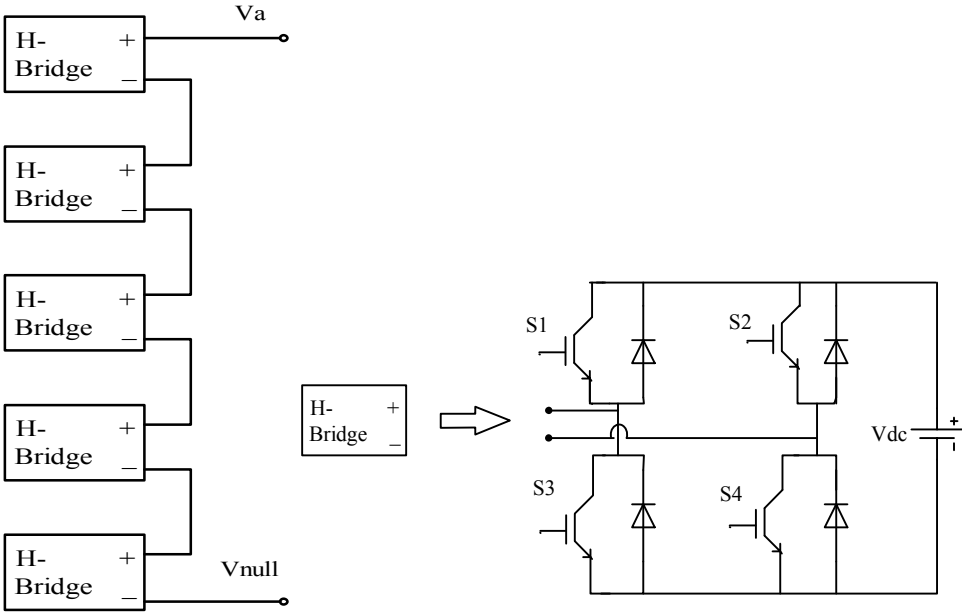

Figure. 1 Structure of eleven level cascaded H bridge MLI

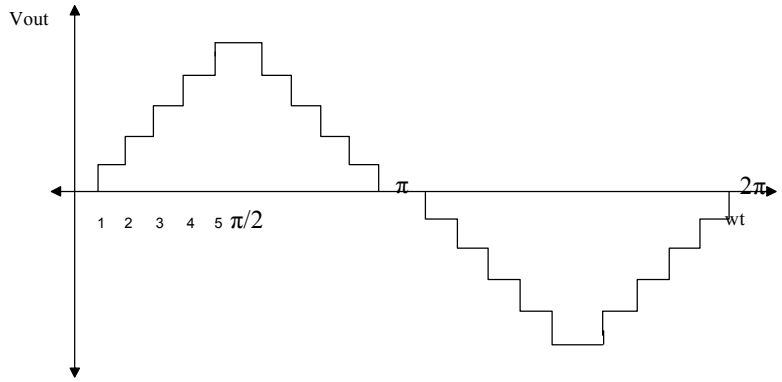

Figure.2 Output voltage waveform of 11-level cascaded MLI

III. SELECTIVE HARMONIC ELIMINATION

The problem of instability takes place in converters due to the harmonics which are integral multiples of the fundamental frequency. There are diverse modulation techniques in fundamental switching frequency available for MLIs such as sinusoidal PWM, Space Vector PWM, and SHEPWM [7]. Space vector PWM and sinusoidal PWM fail to succeed with non equal sources. The promising modulation scheme for the cascaded MLI with unbalanced dc sources is staircase modulation with selective harmonic elimination. Here a specific order harmonics are selected and are minimized to its minimum level or are eliminated from the output voltage waveform. This method is also called fundamental switching frequency based on harmonic elimination theory.

A11-level inverter output voltage waveform is shown in Figure 2. It has five switching angles θ1, θ2, θ3, θ4 and θ5. The non-equal dc sources are Vdc1 to Vdc5.Taking into consideration the waveform characteristics of odd and half-wave symmetry, the Fourier series expansion of the generalized stepped voltage waveform for unequal dc sources is given as follows:

$$V(\omega t)= \sum_{n=1}^{\infty} \frac{4}{n\pi}(Vdc1(\cos n\theta 1)+ Vdc2(\cos n\theta 2)+Vdc3(\cos n\theta 3)+\ldots+Vdcs(\cos n\theta s))\sin n\omega t) \quad (1)$$

The switching angles θ1-θs must satisfy the following condition:

$$0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \leq \theta_4 \text{---} \leq \theta_s \leq \frac{\pi}{2}\ldots. \quad (2)$$

Where S is the number of H Bridges

The number of harmonics to be eliminated from the output of the inverter is S-1. Therefore using 11-level inverter with 5 dc sources, 4 harmonics can be eliminated and the transcendental equations to be satisfied are as follows

$$K_1\cos(\theta_1)+K_2V_{dc2}\cos(\theta_2)+K_3V_{dc3}\cos(\theta_3)+K_4V_{dc4}\cos(\theta_4)+K_5V_{dc5}\cos(\theta_5)=M*S$$

$$V_5=\frac{4}{5\pi}[V_{dc1}\cos(5\theta_1)+V_{dc2}\cos(5\theta_2)+V_{dc3}\cos(5\theta_3)+V_{dc4}\cos(5\theta_4)+V_{dc5}\cos(5\theta_5)] = 0$$

$$V_7=\frac{4}{7\pi}[V_{dc1}\cos(7\theta_1)+V_{dc2}\cos(7\theta_2)+V_{dc3}\cos(7\theta_3)+V_{dc4}\cos(7\theta_4)+V_{dc5}\cos(7\theta_5)] = 0$$

$$V_{11}=\frac{4}{11\pi}[V_{dc1}\cos(11\theta_1)+V_{dc2}\cos(11\theta_2)+V_{dc3}\cos(11\theta_3)+V_{dc4}\cos(11\theta_4)+V_{dc5}\cos(11\theta_5)] = 0$$

$$V_{13}= \frac{4}{13\pi}[V_{dc1}\cos(13\theta_1)+V_{dc2}\cos(13\theta_2)+V_{dc3}\cos(13\theta_3)+V_{dc4}\cos(13\theta_4)+V_{dc5}\cos(13\theta_5)] = 0 \quad (3)$$

where V_1 is the fundamental voltage and V_5, V_7, V_{11} and V_{13} are target harmonic voltages to be eliminated. For three-phase power system applications the elimination of triplen harmonics is not essential as they get cancelled from line-line automatically. To obtain optimum switching angles the modulation index M, is defined to be a representative of V_1.

$$M = \frac{V_1}{4sV_{dc/\pi}};\ 0 \leq M \leq 1 \quad (4)$$

$$\text{and } V_{dc} = V_{dci}/K_i,\ i=1,2,..5 \quad (5)$$

Where, M is the Modulation Index and its value lies between 0 and 1 to cover different values of V_1 which is the required fundamental voltage, V_{dc} is the nominal dc voltage and k1 to k5 are the factors.

IV. ARTIFICIAL BEE COLONY ALGORITHM

Optimization is the mechanism by which one finds the maximum or minimum value of a function or process. There are different methods of numerical optimization techniques such as linear integer, quadratic, nonlinear, dynamic, constraint satisfaction etc. The stochastic search is one among these optimization techniques in which the constraints depend on the random variables. The Evolutionary computing is a guided random search technique &ABC Algorithm falls under this category.

The ABC Algorithm is a population based heuristic algorithm developed by Pham *et al.* [19] and Karaboga [21] independently in 2005. The coordinated food foraging behavior of the honey bees is the basis for this algorithm. The ABC Algorithm features both random global search and an intensified local or neighborhood search. It finds application in finding the optimal solution set among huge sets of probable solutions. It can be used for finding the switching angles as required in the SHE PWM.

The whole colony of bee is categorized into three groups. Depending upon their social responsibilities, they are classified as the employees, the onlookers and the scouts. It is the employee category that brings information, as a result of its search around, regarding the location of the source of food and the quantum of food available. On return to the hive, after collecting the information, the employees express this information in form of exhibiting meaning packed motions, so called a 'dance'. The onlookers add on into an integration depending upon the quantum and quality of the food source. The extend of exploration is controlled and guided or regulated by the scout bees. In a sense the entire team carries out an exploration and exploitation in the search space. The promising solutions to a problem are opted as food sources that are randomly generated. The number of initial food sources is half of the bee

colony. The food source is a *D*-dimensional vector, where *D* is the number of optimization variables. The magnitude of nectar in a food source determines the value of fitness. The employed bees are sent to the food source to determine its fitness. For each food source, there is only one employed bee. So, the number of food sources is equal to the number of employed bees. In addition, the employed bees modify the solutions, saved in memory, by searching in the vicinity of its food source. The employed bees hold memory about the new solution, if its fitness is better than the older one and also share the solutions with the onlooker bees in the hive.

The on-looker bees which are another half of the colony, decide on the supreme food sources using a probability-based selection. Food sources with supplementary nectar attract more on-looker bees. These are sent to the selected food sources that improve the preferred solutions and evaluate its fitness. Similar to employed bees, the on-looker bees keep away a new solution if its fitness is better than an older solution.

The food sources that are not improved for a number of iterations are abandoned. So, the employed bees are sent to find new food sources as a scout bee to replace the abandoned one by the latest. Finally, the elite solution is memorized and is retained for the next iteration. The termination criterion is maximum number of iterations, if it is not satisfied then the algorithm returns to Employed bee phase for the next iteration.

An appropriate fitness function is set to minimize the summation of the individual absolute errors (AE) as given below.

$$\text{Min } FF = 100 \quad \frac{(V1d-V1)^4}{V1d^4} + \left(\frac{50}{V1}\right)^2 \quad \left\{\left(\frac{V5}{5}\right)^2 + \left(\frac{V7}{7}\right)^2 + \left(\frac{V11}{11}\right)^2 + \left(\frac{V13}{13}\right)^2\right\} \tag{6}$$

Subject to the constraint: $0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \leq \theta_4 \text{---} \leq \theta_s \leq \frac{\pi}{2}$

where V1d is the desired fundamental component and 5,7,11, and 13 be the target order of harmonics to be eliminated from the phase voltage.

Steps of ABC Algorithm for the Proposed Work

Step 1: Assign the parameters of ABCA viz. Size of the Bee colony, No. of food sources, maximum cycle number, Initial Switching angles of MLI (be the position of food sources). The fitness value corresponding to the position of each food source is the amount of nectar in the food source.

Step :2 Initialize the position of food sources by randomly generating the switching angles between minimum and maximum limit satisfying eq. (2). It may be noted that more number of food sources result in larger computing time whereas a smaller number of food sources result in a local minima. Hence in this paper the number of food sources is taken as 10.

Step 3: Evaluate the amount of nectar (i.e. fitness value) for each food source using eq. (6).

Step 4: Update the position of food sources and store the food source corresponding to minimum fitness value.

Step 5: Employed bee Phase:
This process would happen for food number times. The size of the food array is No. of food sources × No. of switching angles. For each row of this array, calculate new food position i.e. switching angles from the old one in memory using eq. (7)

$$V_{ij}=X_{ij}+ \Phi_{ij}(X_{ij} - X_{kj}) \tag{7}$$

Where k ∈ {1,2,3……food number} and j ∈ {1,2,3…..D} are indexes chosen at random. D is the no. of optimization parameters which is 5. *X* is the old food position, Φ_{ij} is a random number between [-1, 1].
After computation of each candidate source position V_{ij}, apply greedy selection mechanism

between the older one and the candidate for selecting artificial bee i.e. if the nectar amount of the food source is better than the old source, it is replaced with the old one in the memory. Else the old one is kept in the memory.

Step 6: Onlooker bee Phase:

i)Evaluate fitness value for the artificial bee using eq. (6) and find the probability $Pi = \frac{FF_i}{\sum_{n=1}^{S} FF_n}$, where S is the number of food sources.

ii) Produce the new solutions for the onlookers from the solutions selected depending on Pi.

iii) Apply the greedy selection process as applied in employed bee phase and update the switching angles.

Step 7: Scout Bee Phase:

Keep in track of the set of angles that has not undergone any changes and replace with the new angles randomly and update the main array. In ABCA a position is produced at random and replacing it with the abandoned one. If a position cannot be improved further through a predetermined number of cycles, then that food source is supposed to be abandoned. The value of predetermined number of cycles is a vital control parameter of the ABC algorithm, which is known as ‘‘limit” for abandonments.

Repeat the Employed bee, onlooker bee and scout bee process for the maximum cycle number say 2500. In this work maximum cycle number is considered as stopping criterion. The final tuned value of fitness function parameter would be the global max and the corresponding set of angles would be the global switching angles for which the harmonics would be minimum.

V. RESULTS AND DISCUSSION

5.1 Simulation Results

The optimal switching angles for the proposed 11 level inverter are obtained by writing the coding for ABC Algorithm in MATLAB software on a Intel(R) core i3, 2.4 GHz CPU with memory of 3GB RAM. The parameters chosen for ABC algorithm are as follows.

Size of the Bee colony=20, No. of food sources=10, maximum cycle number=2500, Limit=50.

Various combinations of source voltages and modulation indices are tried and found acceptable and thus validate the proposal. Further a sample case from [13] was considered for fair comparison. The operating voltage (in volts) considered for the five sources are

V_{dc1}= 21.6, Vdc2= 19.6, Vdc3=18, Vdc4=17.2, V_{dc5}=16

Table1 Comparison of THD obtained from ABC Algorithm and PSO

Modulation Index (MI)	Switching Angles obtained from PSO[13] (degrees)					THD (%)	Switching Angles obtained from proposed ABC Algorithm(degrees)					THD (%)
	θ_1	θ_2	θ_3	θ_4	θ_5		θ_1	θ_2	θ_3	θ_4	θ_5	
0.47	37.71	52.81	68.20	86.25	89.40	44.98	12.79	35.79	58.99	87.61	90.0	**14.83**
0.7	16.73	36.03	56.24	62.35	88.37	21.39	11.98	24.17	38.56	59.33	59.49	**13.75**

The optimum switching angles obtained from proposed ABC Algorithm and PSO reported in [13] are presented in Table I for modulation Index of 0.47 & 0.7 respectively. The THD values shown in Table 1 are obtained by measuring the values at the output of single phase MLI. From Table 1 it is shown that

THD is less for ABC Algorithm than PSO .With the proposed method there is a reduction of THD by 67% and 35.7% for MI of 0.47 & 0.7 respectively. THD will get further reduced in three phase MLI due to absence of triplen harmonics.

For the above said five source voltages with 0.8 as the modulation index the optimum switching angles obtained from ABC algorithm are $\theta_{1=}$ 6.7581^{o} ,θ_2 =14.4648 ^{o},θ_3 =23.6551 ^{o},θ_4 = 35.7767 ^{o} and $\theta_{5=}$56.1628 ^{o}. Those switching angles are fed to single phase MLI and the resulting 11 level inverter output and Harmonic Spectrum are obtained which are shown in figure 3. It is observed for this particular case, the lower order harmonics viz. 5th, 7th, 11th and 13th are eliminated with THD of 10.63%.

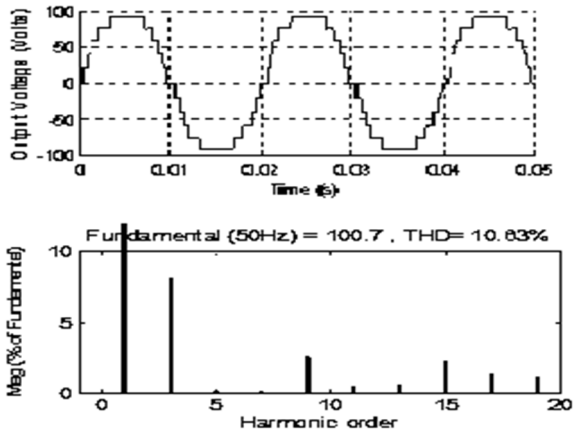

Figure.3 Eleven level stepped waveform and Harmonic Spectrum of MLI with 0.8 as MI

Figure 4 shows the output Voltage waveform and Harmonic Spectrum of MLI with MI as 0.7 in which the above said harmonics are eliminated and THD is 13.75%

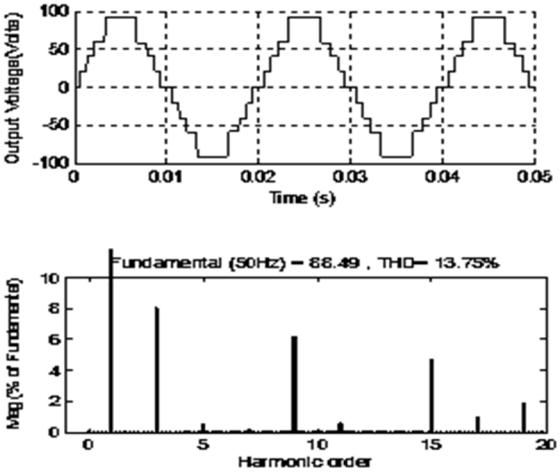

Figure.4 Eleven level stepped waveform and Harmonic Spectrum of MLI with 0.7 as MI

Basically the weightage of the lower order harmonics is heavy in the calculation of the THD. However the fitness function formed does not take into consideration the higher order harmonics and since there is no explicit limitation on the part of the magnitudes of the higher order harmonics it cannot be expected with SHE PWM even as the lower order harmonics are nearly eliminated, that the THD falls to value less than the typically expected 5% level. However there is a reduction of THD and the variation of THD for various modulation indices is shown in figure 5.

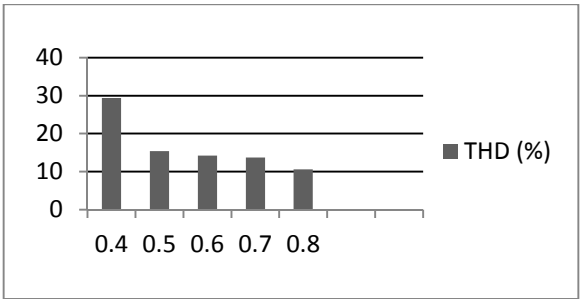

Figure.5 Variation of THD with Modulation Index

The target lower order harmonic contents for varying MI along with THD values are tabulated in Table 2. It is clearly visible that the THD consistently decreases with the increasing modulation index and also the lower order harmonic content (5th, 7th, 11th and 13th) is found to be negligible. The THD is found to be high for lower modulation index of 0.4 and it decreases with increasing MI.

Table 2 Lower order harmonic content and THD for varying Modulation Index

Modulation Index	h5 (%)	h7 (%)	h11 (%)	h13 (%)	THD (%)	V1(Peak) in Volts (Simulation)	V1(Peak) in Volts (Theoretical)
0.4	1.27	0.08	0.03	2.55	29.46	50.35	50.92
0.5	0.94	0.02	1.62	2.63	15.39	62.91	63.66
0.6	0.23	0.38	1.12	0.23	14.23	75.99	76.43
0.7	0.48	0.15	0.56	0.04	13.75	88.49	89.18
0.8	0.13	0.09	0.43	0.52	**10.63**	**100.7**	**101.9**

It can be concluded that with the modulation index of approximately 0.8 the lower order harmonics are almost reduced. The target lower order harmonics with varying MI from 0.4 to 0.8 is plotted in figure 6.From these graph it can be made clear that the lower order harmonics also get reduced with increased modulation indices.

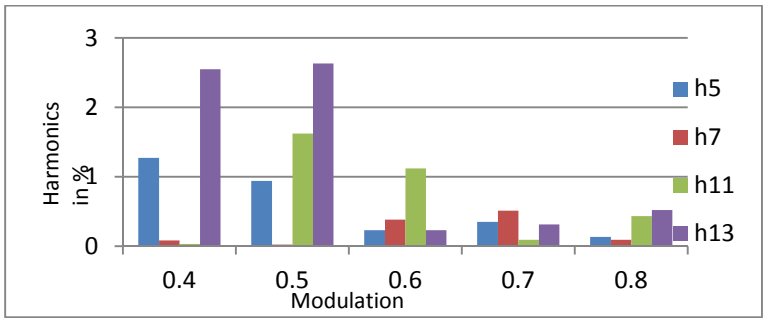

Figure.6 Variation of lower order harmonic content with MI

Implementation of the proposed Method to 11 level CHB using FPGA

In this proposed work FPGA SPARTAN 6A DSP board is used to generate gating pulses for the 20 switches of Eleven level MLI.. This board contains Xilinx XC6SLX25 Spartan 6A DSP FPGA which has

24,051 logic cells. This FPGA has fast 18 x18 embedded multipliers and one 52×18 Kb Block random access memory (BRAM). The synthesis, placement and route are implemented in ISE12.1 environment. Frequency of the clock is 20 MHz. The optimum switching angles are loaded in the FPGA kit using increment/decrement Push button switch Figure 7 shows the RTL schematic of the implementation.

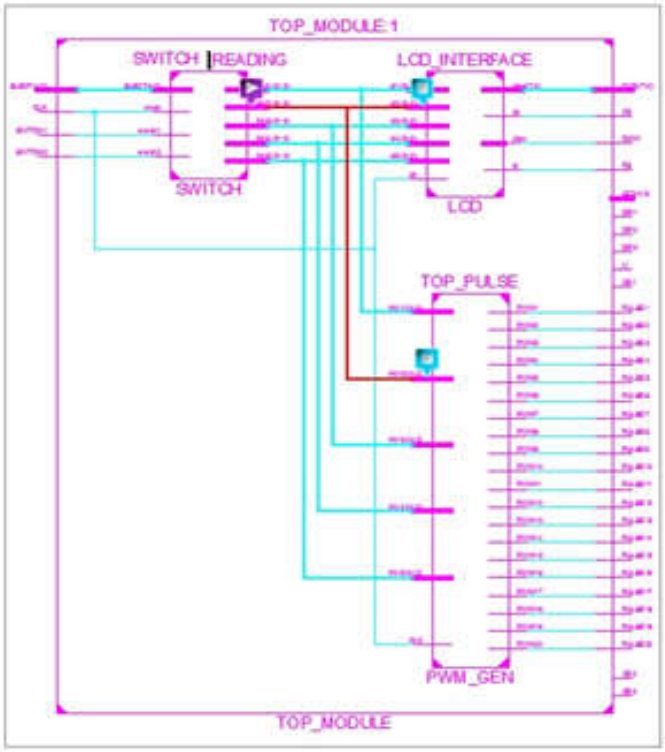

Figure.7 RTL schematic of the implementation

The 'Switch Reading' block receives the switching angles from the increase/decrease switches available in the FPGA kit. The top pulse block generates the gating pulses of required width..The carrier generator is implemented in FPGA using up-down counter. The counter counts from zero to maximum value 'm' and counts down to zero. So, the triangular generator counts a total number of 2m in each half cycle of output period. As the half cycle period is 0.01 Seconds, the count 2m is calculated as

$2m = \frac{20\times10^{-6}}{100}$ which is equal to 2,00,000.

The count m is reduced to 1000 using the expression $\frac{count\times41}{4096}$

Two carrier waves are generated. One is for the switches conducting during positive half cycle and another carrier phase shifted by 180° is for the switches conducting during negative half cycle .It is shown in Figure 8

Figure.8 Carrier waves used for the generation of Gating Pulses

The switching angles $\theta_1..\theta_5$ are converted into constants as follows so that it can be compared with the carrier

$$\text{Constant} = \frac{\theta \times 1000}{90^\circ} \quad (8)$$

The Modelsim output of the gating pulses for the 20 switches of MLI for the modulation index value of 0.8 is shown in Figure 9

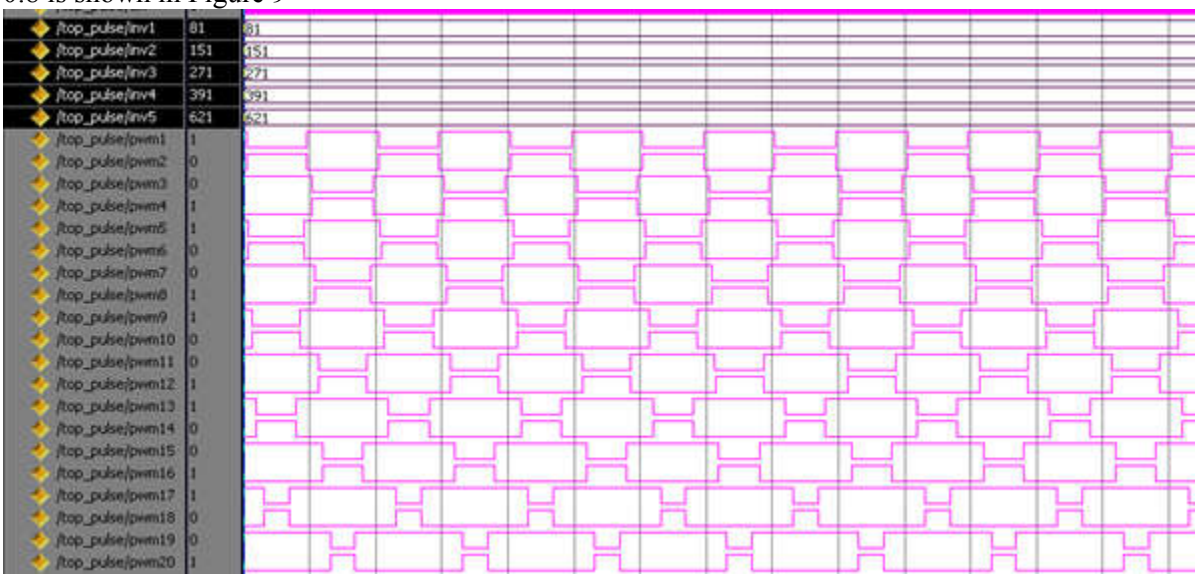

Figure.9 Gating pulse output from Modelsim for the 20 switches of MLI with MI as 0.8

To verify the performance of the proposed algorithm a hardware is built for 11-level cascaded MLI as shown in figure 10.Five Insulated gate Bipolar Transistor modules are used as five H Bridges. Non equal dc sources Vdc1… Vdc5 are given from regulated power supply units. A resistive load of 500 Ω, 3A is connected. For the modulation Index of 0.8 and 0.7, output Voltage is measured and the harmonic spectrum is analyzed using Fluke Power quality analyzer and the THD is found to be 7.9% and 13.5 % with MI of 0.8 and 0.7 respectively. The lower order harmonics are almost eliminated which is evident from figure 11 and 12.Hence the experimental output confirms the validity of the simulation results reported in Table 2.

Figure.10 Experimental Setup of Eleven Level Cascaded MLI

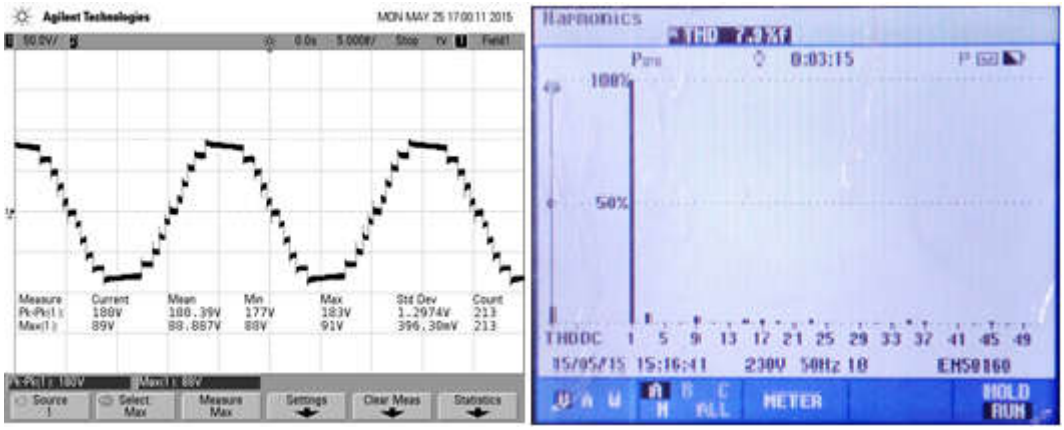

Figure.11 Inverter output voltage & harmonic spectrum for MI = 0.8

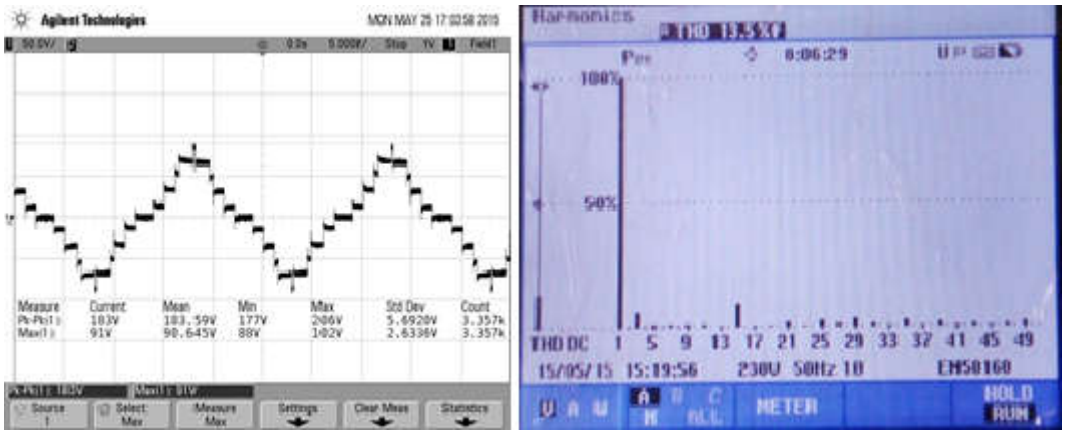

Figure.12 Inverter output voltage & harmonic spectrum for MI = 0.7

VI. CONCLUSION

A methodology for the estimation of optimum switching angles of eleven level cascaded H Bridge MLI with five non equal DC sources using ABC Algorithm is proposed in this work. This algorithm is developed using MATLAB software and the eleven level MLI has been implemented for the optimal switching angles obtained from ABC Algorithm using MATLAB SIMULINK environment. It has been demonstrated that the target lower order harmonics 5th, 7^{th} 11^{th} and 13^{th} order have been well mitigated. The results revealed that the ABC Algorithm adopted in this application is competitive to other popular optimization techniques with some additional advantages like more probable to attain global solution and easy implementation in MATLAB. Further the hardware is built for 11 level cascaded MLI and gating pulses are generated using FPGA Spartan 6A DSP .The experimental output confirms the validity of the simulation results.

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