A QUASI Z-SOURCE NETWORKS FOR MULTILEVEL CONVERTERS BASED ON FUNDAMENTAL PHASE SHIFT COMPENSATION WITH A FAULT-TOLERANT STRATEGY

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Abstract— In this paper, a fault tolerant strategy based on fundamental phase shift compensation with Quasi Z-source networks is proposed. This proposed fault tolerant scheme contains a Quasi Z-source Cascaded H-bridge (CHB) converter, a modified Pulse Width Modulation based control Fundamental Phase Shift Compensation (FPSC) method. The modified implementation of the FPSC method that leverages the flexibility provided by the impedance source CHB converter to generate balanced line-to-line voltages with the amplitudes equivalent to the pre-fault. The control method for the impedance source CHB that incorporates the shoot-through into the operation of the converter which reduces the voltage stress and perform flexible operation. The simulation model of three phase multilevel converter with Quasi Z-source networks is done using MATLAB.

Index Terms— *fault-tolerant inverter, quasi Z-source network, cascaded H-bridge inverter, fundamental phase shift compensation.*

I. INTRODUCTION

Now a day‟s many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation [1-3].Their superior characteristics over the conventional inverters involves higher efficiency, lower switching voltage stress [5]., frequency response characteristics [4]., and lower total harmonic distortion (THD) [6]. In MLCs, the operation of the whole system can be broke and interrupted as they use more number of switches than the conventional inverter [7-9]. Remarkably, addressing the fault-tolerant operation of MLCs releases a new research section due to this. Conversely as the number of inverter voltage levels increases, the number of power electronic switches required for the power stage design increases consistently which leads to both higher cost and lower reliability of the inverter. Alternatively, the reliability of an inverter is fundamental to necessities of a commercial or industrial power application which requires uninterruptable operation. Consequently, the study of operation of multilevel inverters in faulty conditions and familiarizing fault-tolerant control schemes is very important.

In literature, the developed fault-tolerant methods are classified into two categories: During post-fault operation the hardware based remedy method is used and another method is done by modifying the control algorithm [11-13] or the modulation method [14] to reinstate the operation of the MLC. Under fault condition, some methods include additional hardware and modify the topology. They also modify the software, principally the modulation strategy. The Cascaded H-bridge (CHB) converters are predominantly well suited for hardware-based techniques due to their flexible topology and cell redundancy. Fault-tolerant scheme based control depending on FPSC [15] is presented. FPSC method modifies the phase angle of the converter phase voltages to generate balanced line- to- line voltages though; it hinders the natural elimination of the third order harmonics and thus depreciates the line voltage THDs. Sensing a fault, locating the fault and formerly taking proper action is the base to control fault-tolerant problems. Providentially, many fault detection methods have been came out over the last few years. Hence, the main challenge

in this paper is limited to take right action.The low frequency harmonic elimination PWM is proposed in through detailing the relationship of voltage and current ripples with ZS capacitance, inductance, shoot-through duty ratio, and modulation index. The impedance source network can be easily merged with the cascaded H-bridge converters to have enough wider output voltage range and several other advantages.

This proposed design delivers a Quasi Z- source CHB converter that offers the tractability beyond a conventional CHB converter which will be clouted during the post-fault condition. A modified Pulse Width Modulation (PWM) control based method for the Quasi Z-source CHB that incorporates the shoot-through into the operation of the converter. The FPSC method clouts the tractability afforded by the Quasi impedance-source network Cascaded H-bridge to generate balanced line-to- line voltages equivalent to the amplitudes of the pre-fault condition.

The organization of the paper is as follows: Section II delivers circumstantial information about the converter topology. Sescheme and the fundamental of phase shift compensation. Section IV describes the simulation and results of the proposed fault-tolerant strategy for seven level Z- Source CHB. Section V concludes this paper.

II. GROUNDWORK

A).Converter topology: The cascaded H-bridge inverter has pulled in gigantic intrigue on account of the more noticeable demand of medium-voltage high-control inverters. This inverter has one sort of central focuses as the DC-interface voltage in each inverter module is steady and low harmonic distortion. The H-bridge multilevel inverter requires different disconnected dc supplies, which feeds a H-bridge control cell. The CHB multi-level inverter uses capacitors and switches and requires less number of sections in each level. The mix of capacitors and switches consolidate is known as a H-bridge and each cell can give the three different voltages like $+V_{dc}$, $- V_{dc}$ and zero. The quantity of line voltage levels relies upon the modulation index and the given harmonics are to be eliminated. Contrasting and other customary inverter frameworks, multilevel inverter frameworks has the points of interest that the lower harmonic components on the output voltages can be dispensed with and EMI issue could be diminished. In this way, CHB converters are amazing topologies for planning fault tolerant reversal stages.

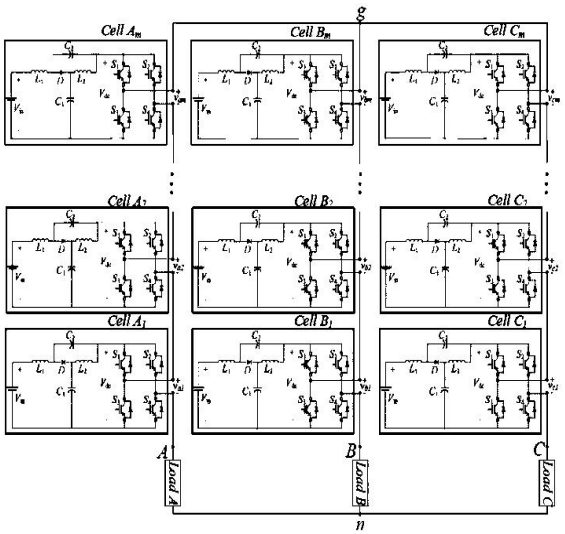

Figure 1: A Three- Phase n- level QZSI-CHB converter with M- series connected H- bridge cells in each phase

Voltage-fed ZSI structures like QZSI, can be promptly joined with the CHB topology to improve its fault tolerant properties. The topology of the seven-level quasi Z-source inverter comprises of a progression of single stage H-bridge inverter units, quasi Z-source impedance systems and DC voltage sources, DC sources. The QZSI expands a few preferences over the ZSI, for example, constant current from the input DC source, cut down component ratings

and upgraded reliability. In this work a QZSI organize is coordinated into the CHB converter topology to gather a fault tolerant CHB converter with a high level of adaptability. The QZSI organize is extraordinarily chosen because of the lower voltage rating prerequisite for its capacitors contrasted with the conventional ZSI network. As Fig. 1 outlines the circuit diagram of the n-level QZSI based CHB converter, can be referred to as the QZSI-CHB converter hereinafter. The proposed QZSI-CHB converter puts a QZSI network on the input side of every standard H-bridge cell. Each period of the QZSI-CHB converter is comprised of m QZSI cells (n=2m+1).There are two methods of activity of a Quasi Z-source inverters.

- Non-shoot through mode (active mode)
- Shoot through mode

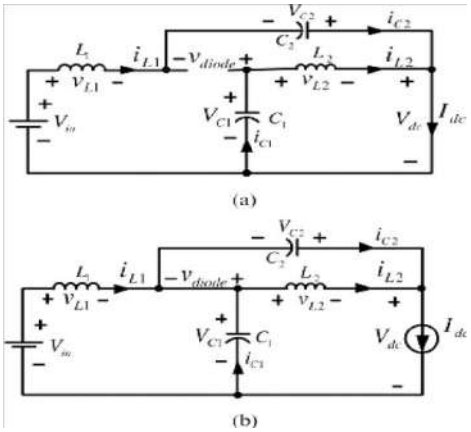

Figure 2: Modes of Operation
(a) Shoot through Mode (b) Non- Shoot through Mode

In the non-shoot through mode, the exchanging design for the QZSI is like VSI cell while additionally boosting the input voltage to its H- bridge stage.

$$V_{dc} = B \times V_{in} = \{1/(1-2D)\} \times V_{in}$$

where D is the shoot-through duty ratio, B is the boost factor of the QZSI network, Vin is the input voltage to the QZSI cell and Vdc is the input voltage to the H-bridge phase of the QZSI cell (see Fig. 2). At the point when a QZSI cell is in a shoot-through mode, the input terminal to the H-bridge organize is short circuited, rendering the estimation of Vdc to zero. In this mode, switches of a similar stage in the inverter bridge are exchanged on momentarily for a brief span. The source all things considered does not get short circuited when tried to do on account of the nearness of LC network while boosting the output voltage. The DC link voltage amid the shoot through states, is helped by a boost factor, whose esteem relies upon the shoot through duty ratio for a given modulation index. In a shoot-through mode, the output terminal voltage of the QZSI cell is constantly equivalent to zero. However, the output terminal voltage can be equivalent to V_{dc}, 0, or - V_{dc} in light of the status of conduction of the switches in the H-bridge stage.

B) *Modulation Method:* A specific carrier based PWM technique, called Phase Shifted PWM is exceptionally appropriate to actualize the proposed fault tolerant system. For this work, the PS-PWM technique is adjusted somewhat to produce shoot-through switching states notwithstanding customary non-shoot-through states. The customary PS-PWM uses two carrier signals with 180° phase shift for each H-bridge cell in a CHB converter. The relative phase angle of carrier signals for each period of the converter relies upon the quantity of H-bridge cells in each stage. To create the shoot-through states utilizing the changed PS-PWM procedure, another shoot-through signal with adequacy of 1-D is presented. In a common ZSC inverter, the abundancy of the produced voltages can be expanded by expanding the length of the shoot-through states. Notwithstanding, expanding the shoot-through prompts an expansion in the output voltage of the ZSI hardware (the Vdc in Fig. 1). This dc link voltage is the voltage stress that the inverter switches need to endure. Hence, while expanding the abundancy of the generated

voltages utilizing shoot-through states, it is fundamental to guarantee that the sufficiency of the dc link voltage does not surpass the stress rating of the switches. faulty phase can just create a voltage with a greatest amplitude of 2Vdc (2 p.u.).The FPSC system adjusts the phase angles of the inverter phase voltage ($è_{ab}$, $è_{bc}$, $è_{ca}$) to produce adjusted line-to-line voltages. Adjusting the phase angles of inverter voltages can prompt adjusted line-to-line voltages for a 7-level QZSI-CHB converter with one skirted faulty cell.

III. FAULT-TOLERANT STRATEGY

The issue of detecting a fault, finding the area and afterward making suitable action is the premise of fault tolerant control. Be that as it may, the principle challenge in this paper is constrained to make suitable action after fault determination. In this paper, it is accepted that the type and location of the fault has been identified by the proposed strategy. In this segment, a fault tolerant procedure for a QZSICHB converter in light of FPSC strategy is proposed. The proposed fault tolerant methodology consolidates the voltage gain flexibility furnished by the QZSI-cells with the phase shifting property of the FPSC technique to completely recuperate the converter endless supply of single or numerous faults on inverter switches.

The proposed fault tolerant methodology works in two phases to adjust for the defective switches in the inverter. The main stage includes bypassing the defective cells while the second stage includes applying the FPSC method to recuperate the amplitude and adjust the phase angles of the inverter voltages. On the off chance that there are at least one defective switches in a QZSI-CHB converter, in view of the fault type and the location of the faulty switches, the faulty QZSI-cells neglect to create the greater part of the previously mentioned feasible output terminal voltage levels in a non-shoot-through mode (Vdc, 0, - Vdc). Subsequently, the inverter stages with flawed cells can never again produce phase voltages that are symmetric around the zero volt level. In its first phase of task, the proposed technique sidesteps the majority of the defective QZSI cells. Be that as it may, in this condition the amplitude of the voltages produced by the converter are never again equivalent. For example in a 7-level QZSI-CHB converter with one faulty cell, the healthy phases can produce voltages with a most extreme amplitude of 3Vdc (3 p.u.) while the

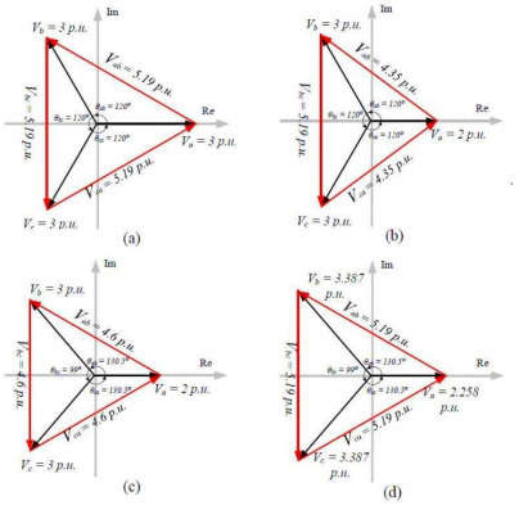

Figure. 3. The phasor diagram of phase voltages in a QZSI-CHB converter: a) The healthy operation, b) The faulty condition in which the faulty cell is bypassed and the line-to-line voltages are unbalanced, c) The phase angles are modified according to the FPSC methodology to produce adjusted line-to-line voltages with less voltage diminishment, d) The voltage gain is altered by changing the shoot-through ratio to compensate for the line-to line voltage reduction in the post-fault condition.

The outcome of the phase angles in balanced line-to-line voltages can be created by resolving the following set of equations for $è_{ab}$, $è_{bc}$ and $è_{ca}$,

$V_a^2 + V_b^2 - 2V_aV_b \cos(\theta_{ab}) = V_b^2 + V_c^2 - 2V_bV_c \cos(\theta_{bc})$

$V_b^2 + V_c^2 - 2V_bV_c \cos(\theta_{bc}) = V_c^2 + V_a^2 - 2V_cV_a \cos(\theta_{ca})$

$\theta_{ab} + \theta_{bc} + v_{ca} = 360^0$

where V_a, V_b and V_c are the amplitude of the phase voltages later circumventing the faulty cells, in 7-level QZSI-CHB converter with one evaded cell (the bypassed phases is phase "a"), substituting V_a = 2 p.u. and $V_b = V_c$ = 3 p.u. yields $\theta_{ab} = \theta_{ca}$ = 130.5 and θ_{ba} = 99. The phase angles of the inverter phase voltages can be effortlessly accustomed in PS-PWM through altering the phase angles of the reference signals.

Even though by relating the FPSC technique to a QZSI-CHB converter with faulty cells balanced line voltages can be created, yet, the converter operation is not completely improved because the amplitude of the generated line-to-line voltages are fewer than those of a healthy converter. In the 7-level QZSI-CHB converter the amplitude of the line-to-line voltages afore fault existence is equal to 5.19 p.u., subsequently use of the FPSC the amplitude of the line-to-line voltages is compact to 4.6 p.u. The proposed method in this work, influences the flexibility provided by the shoot-through states in a QZSI circuit to entirely pull through the amplitude of the line voltages to their pre-fault condition. To make progress in the line voltages, the planned method upturns the post-fault inverter voltage gain (R_{fault}) to,

$$Rfault = R\ pre\text{-}\ fault / ST$$

where $S_T = |VLL|_{fault} / |VLL|_{pre\text{-}fault}$

where $R_{pre\text{-}fault}$ is the inverter voltage gain before fault occurrence and S_T is a performance reduction factor. $|V_{LL}|_{fault}$ and $|V_{LL}|_{pre\text{-}fault}$ are the amplitudes of the line-to-line voltages of the inverter post and pre-fault condition, correspondingly.

IV. SIMULATION AND RESULTS

This division affords results generated through exploiting the proposed fault-tolerant scheme to reestablish the operation of a prototype seven-level QZSI-CHB converter to the pre-fault conditions. Each Z-Source system is coupled to a 12 V battery. The Quasi Z-Source modules are C1 = C2 = 2200 ìF, and L1 = L2 = 500 ìH. The output terminals of the QZSI-CHB converter are linked to a three-phase inductive load with a 0.9 power factor accumulated using a 7 Ù resistor in series with a 1.2 mH inductor in each phase. In the operative point
used for producing the results (V_{load} = 44 V, I_{load} = 6 A), in order to lessen the voltage stress on the switches, the modulation index and the shoot-through ratio are set to 0.85 and 0.15, in turn. The voltage gain in normal operation is found as 1.21. The fundamental and switching frequencies of the PS-PWM method are 50 Hz, and 2 kHz; correspondingly.

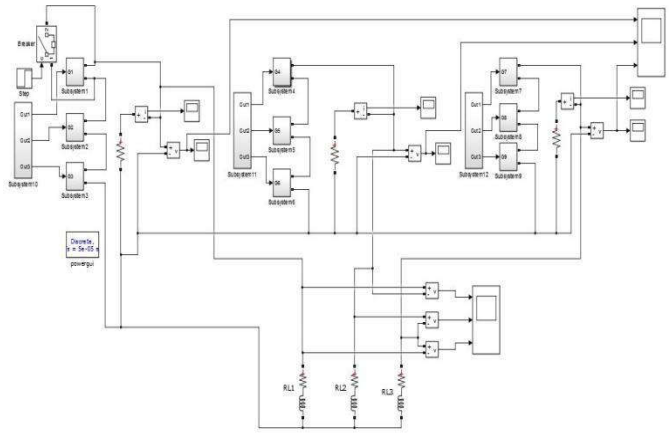

Figure. 4. Simulink Model

The THD of the load voltages is calculated as 9.5%. Evaluating the occurrence of a single fault in phase „a", the faulty cell is bypassed at the first. Consequently, the number of operative cells in phase „a" is compact to 2 cells. To generate balanced line-to-line voltages, created on the phase shifts between the inverter phase voltages need to be adjusted to a = = 130.5°.

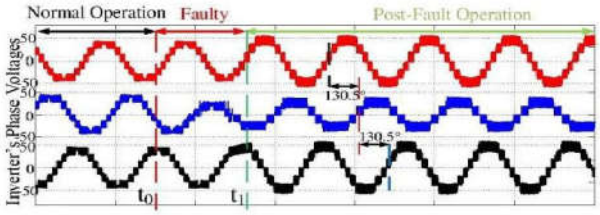

Fig.5 (a)

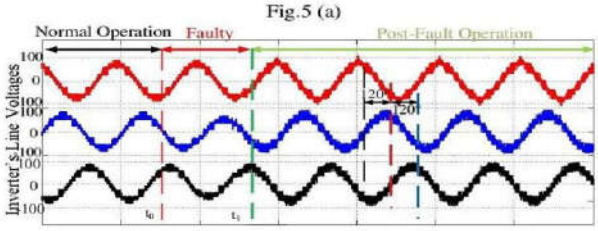

Fig.5 (b)

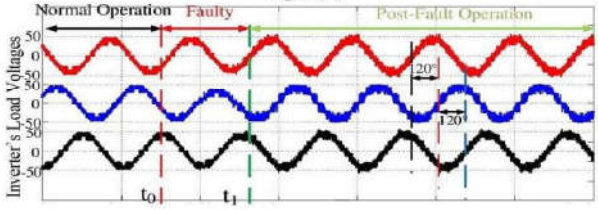

Fig.5 (c)

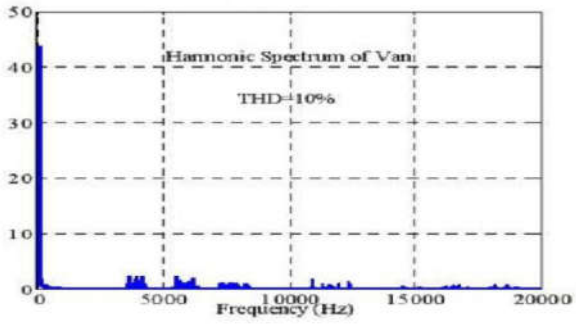

Fig.5 (d)

Figure. 5. The QZSI-CHB"s voltages in the event of a single faulty switch in phase „a". (a) Inverter"s phase voltages, (b) line-to-line voltages, (c) load voltages, (d) the harmonic spectrum of the load voltage V_{an}. To rival the fault condition, one of the switches in phase 'a' of the inverter was automatically short circuited at $t = t_0$.

Successively, the H-bridge cell comprising the faulty switch was circumvented and the proposed fault tolerant approach was applied at t = t1. The generated phase voltages of the converter throughout the fault retrieval period ($t_0 \leq t \leq t_1$), and the post-fault operation ($t \geq t_1$). The amplitude of the phase „a" voltage is equal to 35.1 V,

while the amplitude of the voltages in the vigorous phases „b‟ and „c‟ are equal to 52.55 V and 52.6 V, individually. By the side of this point ($t \geq t_1$) ,the proposed fault-tolerant stratagem is initiated to reestablish the action of the converter to the pre-fault conditions.

V. CONCLUSIONS

In this paper, another fault tolerant methodology for enhancing the execution of a QZSI-CHB converter under defective condition was proposed. Utilizing the proposed technique, just the defective QZSI cell was skirted and the staying healthy cells were operative to utilize the most extreme limit of the converter. By embracing the FPSC strategy, rather than simply expanding the voltage gain in the broken stage, the voltage gain of all the operative cells were expanded equitably to limit the voltage stress over the sound switches. The proposed methodology can be effortlessly actualized on any multilevel inverter with a consolidated Z-Source network without constraint on the system topology or the quantity of inverter voltage levels.

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