A NOVEL NINE LEVEL REDUCED SWITCH MULTILEVEL INVERTER

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Abstract— in this paper, a symmetric nine-level inverter is proposed. The inverter employing only one input source and fewer components. It makes full use of the conversion of series and parallel connections of one voltage source and two capacitors to realize nine output levels, thus lower THD can be obtained with HFM methods. In previous years MLIs using more than one voltage source and power devices and also the size of the device is also large. The voltage stress on power devices is relatively relieved, which has broadened its range of applications as well. The nine level inverter is having the inherent self voltage balancing ability. The theoretical analysis and simulation results confirm the feasibility of proposed symmetric nine-level inverter.

Keywords*— nine level inverter, one voltage source, two capacitors, self-voltage balancing.*

I.INTRODUCTION

Dc to ac power conversion is a key technology in the modern set-up of generation, transmission, distribution, and utilization of electric power. High frequency ac power distribution system (HFAC PDS) proposed in has become an alternative because of its merits such as fewer conversion stages, higher efficiency, faster response, high power density, distributed heat profile and potential for connector-less power transfer. The basic concept of an MLI to achieve high power is used by semiconductor devices along with lower voltage power conversion and produce staircase output waveform. HFAC PDS is usually having two stages: source side high frequency multilevel inverter and load side ac/ac voltage regulation module. The voltage stress on the power devices is much lower as compared to the operating voltage. Thus a higher voltage waveform can be obtained with comparatively low voltage rated switches. To connect multiple resonant inverters in series or in parallel to increase the power capacity and also control of both amplitude and phases will become complicated .The main advantages of MLI are output waveform quality increase ,low switching loss, low voltage stress, good electromagnetic interference and total harmonic distortion.

A HF MLI is used to transform the dc voltage source from the batteries, fuel cells or photovoltaic cells into a HF staircase output then simplifying the design of output filters. However, the level number is restricted by the complexity of the MLI. The output frequency of the HF inverter usually ranges from 400 Hz to 50 kHz. Based on the output waveform the inverter can be classified into square wave inverter, quasi-square wave inverter, multilevel inverter and two level pulse width modulation inverter. Traditional MLIs include the neutral-point-clamped inverter, flying-capacitor inverter and cascade H-Bridge inverter. The NPC and FC inverters respectively use diodes and capacitors to clamp the voltage levels and more levels can be obtained by increasing the number of power devices.

However, both the circuit conFigureurations and their controls will become extremely complicated along with the increasing number of voltage levels. Additionally, the capacitors' imbalance is another problem needed to be solved. The CHB inverter increases the output voltage levels and simplifies the modulation by the combination of H-bridge cells.

II.SWITCH TECHNOLOGY

A.REDUCED SWITH MULTILEVEL INVERTER

The multilevel inverter does have some disadvantages. One particular disadvantage is the great number of power semiconductor switches needed and also it needs separate DC sources. There are many topologies to reduce the switches in the multilevel inverter. The bi-directional switch topology is used for the reduction of switches. There are three types of bidirectional switch topology such as common collector type, common Emitter type and Diode Bridge Topology. This project uses the reduction of Switches and voltage Sources.
The proposed basic unit comprised of one voltage source and nine unidirectional switches. The proposed topology consists of two stages.

The first stage is developed SC circuit which is different from basic sc cell it can output more voltage level relatively fewer components. The second stage is the H-bridge circuit is used to change the polarity of the first stage output. Topology is exactly when the high frequency modulation MLIS are receiving much more and wider attention both in terms of topologies and control schemes. A grid connected converter topology was proposed with only one voltage source, a flying capacitor and eight switches. The output of nine level inverter strategy keeps the capacitor voltage at a desired level such as1/3 v dc. The low voltage rated switches used in MLI, each switch requires a related gate driven circuit, protection circuit and heat sink. This may cause the overall system to be more expensive, complex and bulky. In the past few years effort being directed to reduce the power switches count in MLIs. This topology having their own merits and demerits. This paper aims at presenting a review of MLI topologies proposed with the exclusive objective of reducing the power switch count
.

B. Multilevel DC to AC Conversion

An inverter is electrical device which is used to convert direct current in to alternating current using some switches and control circuit .The inverter function is totally opposite to the rectifier. There are many differ tent types of inverter are used .Some of the inverters are multilevel inverter, modified multilevel inverter, pure sine wave inverter, solar inverter. Now we are discuss about MLI .Multi level inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. The concept of the multilevel inverter is a modification of two level inverter. In MLI two voltage levels are combined together and produce the output at with lower dv/dt and lower harmonic distortion. The smoothness of the waveform is proportional to the voltage levels. .The level of the waveform is increased means the waveform is smoother but the complexity is increased. The multilevel inverter is having three topology

III.PROPOSED NINE LEVEL INVERTER

A.PWM CONTROL

Pulsewidthmodulation is a modulation technique used to encode a message into pulsing signal. The simplest way to generate a PWM signal is the interceptive method which requires saw tooth or a triangular waveform and a comparator. There are three types of PWM .This paper sinusoidal pulse width modulation method is used.

B.SINUSOIDAL PULSE WIDTH MODULATION

sinusoidal PWM is a type of “carrier based” pulse width modulation .carrier based PWM uses pre-defined modulation signals to determine output voltages.in sinusoidal PWM,the modulation signal issinusoidal,with the peak of the modulating signal always less than the peak of the carrier signal.sinusoidal PWM inverter leg and line-line voltages are illustrated below.The difference between two level and multilevel inverter is number of carriers are used in multilevel SPWM.for ‘m’level inverter ‘m-1’carrier are used .interaction of particular carrier

and reference is used togenerate gating signal for particular complementary pair of switches in diodes clamped inverter

The modulation index of the fundamental waveform

$$M_{of}=1/4\sum_{i=1}^{4}\cos(\Theta_i)$$

Total harmonic distortion of proposed nine level inverter can be expressed as

$$THD=\frac{\sqrt{\sum_{k=3,5...}^{\infty}[\sum_{i=1}^{4}\cos(k\,\Theta i)]^2}}{\sum_{k=1}^{4}\cos(\Theta_k)}$$

IV. IMPLEMENTATION

A. NINE LEVEL VOLTAGE WAVEFORM

The proposed inverter has nine output voltage levels: +-2vdc+-3vdc/2, +-vdc, +-vdc/2, 0. Two capacitor are used in this paper the two capacitor are charged and discharged in series at levels + or - V_{dc} and + or – $2V_{dc}$ in this interval they share same amount of charging and discharging current. At 0 levels the capacitor voltage remains unchanged. The proposed topology using independent capacitor. Load is inductive means the current will flow in opposite direction

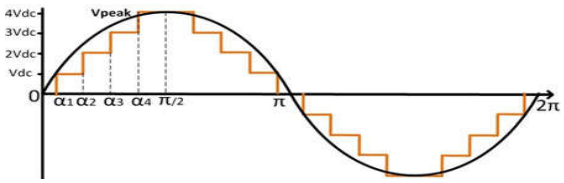

Figure 1: nine level voltage waveform

B. BLOCK DIAGRAM

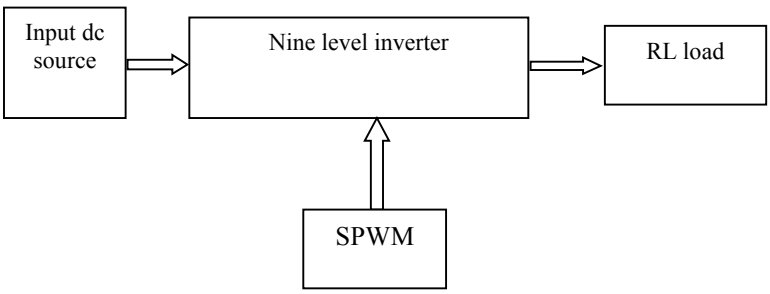

Figure 2: block diagram

An input DC source is given to the nine level inverter which converts different level DC to AC voltage. By using sinusoidal pulse width modulation technique with the comparison of sinusoidal reference signal and triangular carrier signal the control strategies for predicting the switching angle of the switches in the inverter the required output alternating voltage is generated and fed to the RL load. Finally the entire system will provide reduced switching losses and increased performance characteristics.

C.CIRCUIT DIAGRAM

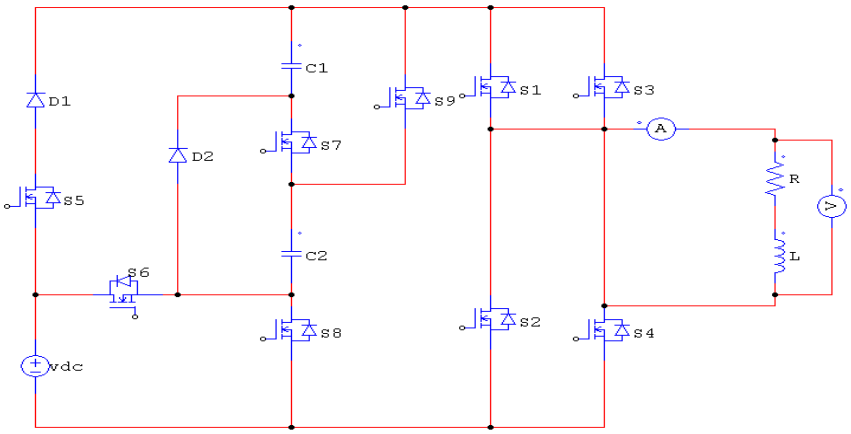

Figure 3: circuit diagram

V.SWITCHING PATTERNS AND STATES OF THE DIODES AND CAPACITOR AT EACH VOLTAGE LEVEL

where symbols of 1 or 0 in the switches columns indicate that the switches are turned on or turned off ,symbols of 1 or 0 in the diode column indicate that the diodes are forward passed or reverse biased ;symbols of C,D or –in the capacitor column indicate that the capacitors are charged ,discharged or unchanged

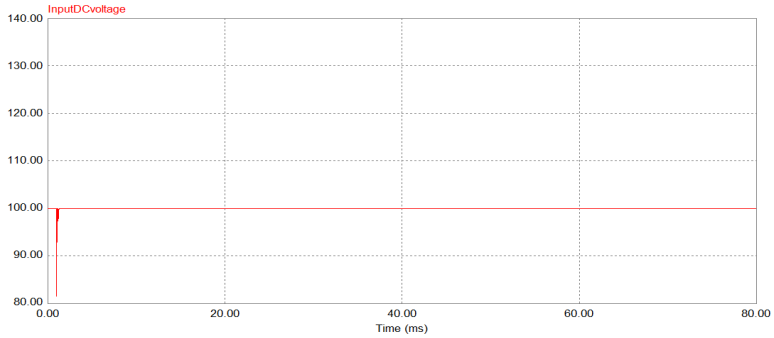

Figure 4: input voltage waveform

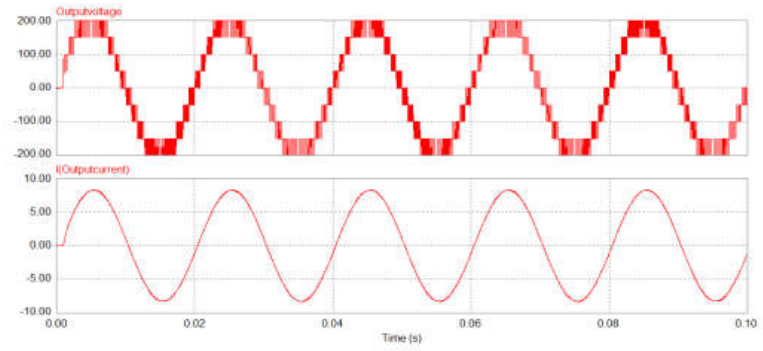

Figure 5: output voltageand current waveform with RL load

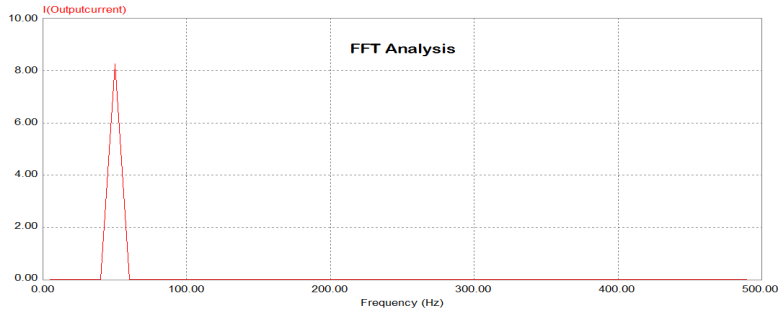

Figure 6: harmonic spectrum

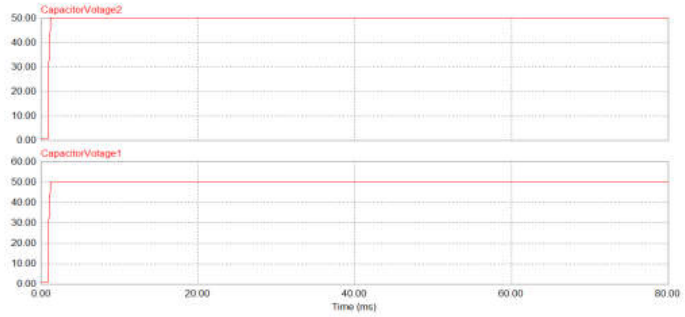

Figure 7: capacitor voltage waveform

Voltage levels	Switches in HBC	Switches in DSCC								Diodes		Capacitor	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	D_1	D_2	C_1	C_2
$2V_{dc}$	1	0	0	1	1	1	1	0	0	0	0	D	D
$3V_{dc/2}$	1	0	0	1	1	1	0	0	1	0	1	D	D
V_{dc}	1	0	0	1	1	0	0	1	0	1	0	C	C
$V_{dc/2}$	1	0	0	1	0	0	0	1	1	0	1	D	D
0	0	1	0	1	0	0	0	1	1	0	0	-	-
$-V_{dc/2}$	0	1	1	0	0	0	0	1	1	0	1	D	D
$-V_{dc}$	0	1	1	0	1	0	0	1	0	1	0	C	C
$-3V_{dc/2}$	0	1	1	0	1	1	0	0	1	0	1	D	D
$-2V_{dc}$	0	1	1	0	1	1	1	0	0	0	0	D	D

Figure 8: .SWITCHING PATTENS OF DIODES AND CAPACITORS

CONCLUSION

Compared with the existing topologies, proposed topology can achieve nine-level staircase output with only one voltage source, fewer power devices and relatively less voltage stress. All these have enlarged its application scopes. Voltage balance problem is avoided by the inherent self-voltage balancing ability, which has simplified the modulation circuits and the lower THD. As a result, the switching loss is significantly reduced. The capacitor calculation and power loss analysis are conducted in this paper, and the comparisons with existing topologies further testify the superiority of proposed HF inverter. All the merits and the feasibility of proposed topology are evaluated by a simulation model and an experimental prototype with rate power of 200W, and their results illustrate that proposed inverter is a preferable topology to implement HF power source for HFAC PDS.

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