BRIDGELESS SEPIC CONVERTER FOR POWER FACTOR IMPROVEMENT

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Abstract

The new path has been laid to improve the power factor which was the major problem faced in our day to day life. There are multiple solution has been raised for the problem but the method which is proposed to be a better one than all others because it reduces the total harmonic distortion drastically and increases the power factor tremendously. The method which is introduced is Bridgeless SEPIC. In this input rectifier is eliminated, Multi loop fashion is introduced for the controller. The outer loop provides the reference current and the inner loop provides pulse for the switches through PI controller. Analytical and practical calculation is done for the proposed system and it is examined with R load. And also a comparative study is made with conventional SEPIC. The proposed system is executed in the MATLAB.

Keywords: *DSPIC2010 MC, bridgeless converter, Power Factor Correction (PFC), SEPIC converter, Total Harmonic Distortion (THD), MATLAB*

1. INTRODUCTION

In the recent trends, the modern devices reduce the burden of the human effects, but it is not so this will lead us into the degradation of the human life in the future. This new power electronics based devices have been increased which brought suffocation of the power because these devices draw excessive power and also introduces a new term called power quality issues where more harmonics are evolved and disturb the quality of the power. Thus the International Electro technical Commission (IEC) 61000-3-2 have drawn margin for this problem by setting limits for the harmonics [1]. This necessitates a power factor corrector for reduction of harmonics. This gives a glimpse about the power factor corrector [2]. In the transmission line, the harmonic and power factor is the two devastating issues. In order to safeguard, the active power factor correction is an upcoming remedy for the solution [3-5].

There are different PFC topologies Boost [6-7], buck-boost [8], Buck [9-11] and SEPIC converter [12-17] and thus paved the way for the novice to understand better in this particular domain. In the boost converter, the output DC voltage is greater than the input AC voltage. Since the boost converter is applied in the practical application because of its larger usage. This gives a detailed view about continuous and discontinuous mode [6-7]. Both buck and boost operation is carried out in the single circuit. This provides better results in the both cases. The input current should be sinusoidal to obtain unity power factor [8]. A buck PFC converter procures for low-voltage applications because the output DC is lesser than the input AC voltage. The buck PFC can obtain high efficiency over the input voltage range. The harmonic range is within the specified limit imposed by IEC 61000-3-2 requirements [1].

The input current in the buck converter is not that much more effective along the end of the cycles. So it required an extensive filter to improve the power factor. There is no compatibility between voltage and power factor. To bring an end to these types of problem, SEPIC or Cuk converter arises because it has high power factor which can be used for a wide range of voltage condition [12-13]. In Cuk converter, the voltage output is inverted so the SEPIC is mostly preferred because of its non-inverting voltage output

[14]. Different topologies have been given to reduce the total harmonic distortion and to increase the power factor [15-17].

This paper presents a new topology and it is named as bridgeless SEPIC AC to DC converter. The section II gives the working of the bridgeless SEPIC. The section III gives theoretically analyze of bridgeless SEPIC. The section IV gives simulation results. The section V hardware analyses of proposed system. The section VI gives conclusions and future scope.

II. Bridgeless SEPIC converter

The bridgeless SEPIC converter is derived from the conventional SEPIC converter. The basic difference between them is a full bridge converter is present in the conventional SEPIC converter. The conventional SEPIC is consist of two stages AC to DC then it is followed by the SEPIC converter (DC to DC). The operation starts with mode 1, when the switch is closed the current path will be an AC supply flow through a full bridge rectifier then it will pass over to the inductor L_1 and final through the switch Q_1. And the remaining half is reversed biased by the diode. The inductor L_2 and inductor C_1 will be at the resonant. The output voltage will be less because it is supported only by the output capacitor C_0. This indicates the buck operation where the output voltage is less than the input voltage. The mode 2, the switch is open and the diode is forward biased. The current path will be AC supply flows through a full bridge rectifier then it will flow L_1, L_2 and that time the capacitor C_1 will start to discharge. The load is directly connected to the inductor during this mode. And this indicates the boost operation where the input voltage is less than the output voltage.

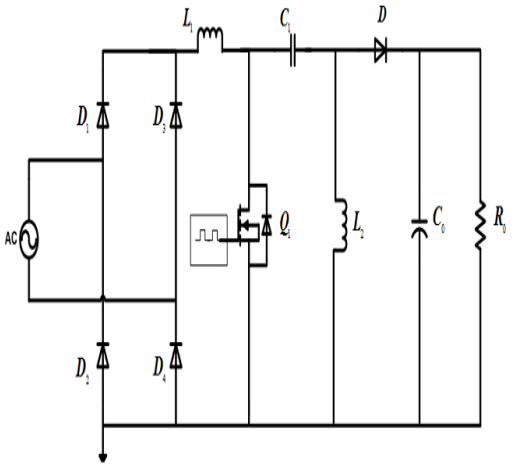

Fig 2.1: General circuit of conventional SEPIC converter

The bridgeless SEPIC converter, the full bridge rectifier is replaced by three switches which differ from the conventional setup. This makes the uncontrolled to controlled system. The working starts when three switches are on, the input inductor current I_{L1} get increased. The voltage of capacitor C_1 is equal to the output inductor voltage. The input voltage will be equal to capacitor C_1 before all the switches turned on. When the switches turn on, the I_{L2} decreases linearly. The switches go to off at the end of this stage. The next stage starts with the end of all switches and the diode start to conduct. The input inductor current began to decline. The current flows through anti parallel diodes in the switches. Finally, the diode gets disconnected and there is no link between the input side and the output side. Since there is no connection between input and output side, the current through the inductor will freewheel inside the input side. And the working of the modes is explained in detail below.

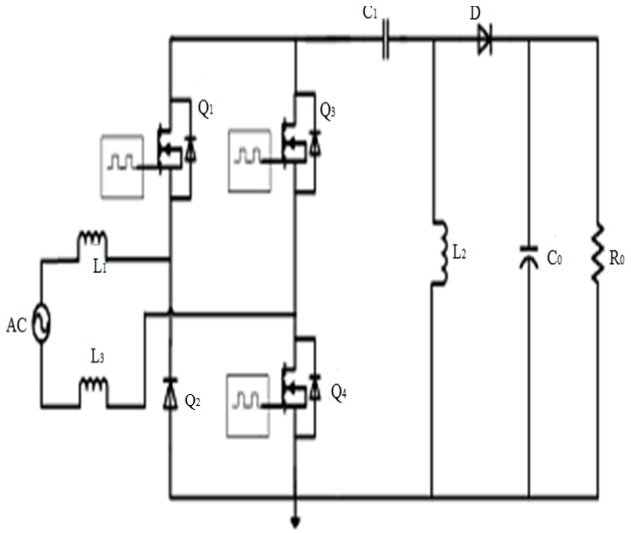

Fig 2.2: General diagram of bridgeless SEPIC converter

2.1 Operation Principle

The circuit consists of two symmetrical structures and in that investigation is mainly done for the positive half cycle. The positive half cycle is divided into three modes,

2.1.1 Mode1:

In this mode, all the switches Q_1, Q_3, Q_4 are turned on. The current path is traced from AC supply to switch Q_1 and then it flows to capacitor C_1 from there it pass through inductor L_2, then its flow through the switch Q_4 and finally L_3 and back to AC supply. The input inductor current start to increase and the output inductor current decrease linearly. The rate of change of the input inductor current and output inductor current is derived by the formula

$$\frac{di_{ac}}{dt} = \frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = \frac{V_{ac}}{L_{1,3}} \quad \rightarrow \quad (1)$$

$$\frac{di_{L2}}{dt} = -\frac{V_{ac}}{L_2} \quad \rightarrow \quad (2)$$

Where $L_{1,3}$ value is given by

$$\frac{1}{L_{1,3}} = \frac{1}{L_1} = \frac{1}{L_3} \quad \rightarrow \quad (3)$$

About the switch Q_3 in this mode is given by the equation

$$i_{Q3} = i_{ac} - i_{L2} = \frac{V_{ac}}{L_{1,3}} + \frac{Vac}{L_2} \quad \rightarrow \quad (4)$$

This mode gets to an end by trading off the switches.

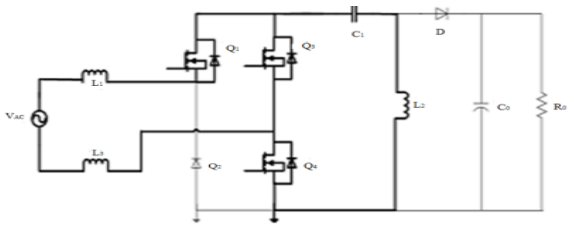

Fig 2.3: Conduction mode1of bridgeless SEPIC converter

2.1.2 Mode 2:

After the turning off the switches Q_1, Q_3 and Q_4, the conduction in Q_1 and Q_4 will take place by the antiparallel diodes. In this mode, the diode D is forward biased and it will support for delivering input current and output current to flow through it. The input inductor current will reduce and the output inductor current starts to increase. The output inductor current is proportional to the input inductor current. The inductor current is given by the formula

$$\frac{di_{L_1}}{dt} = \frac{di_{L_3}}{dt} = \frac{V_{ac}}{L_{1,3}} \quad \rightarrow \quad (5)$$

$$\frac{di_{L_2}}{dt} = \frac{V_{dc}}{L_2} \quad \rightarrow \quad (6)$$

This mode ends by the diode D going to off stage.

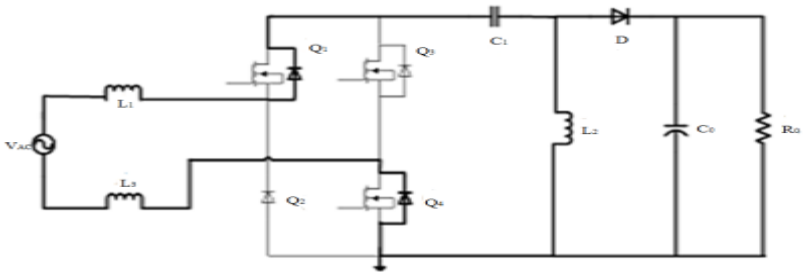

Fig 2.4: Conduction mode 2 of the bridgeless SEPIC converter

2.1.3 Mode 3:

In this mode, Q_1 and Q_4 are conducting through antiparallel diode. The inductor current L_1, L_2 and L_3 are equal, the input voltage Vac and Vdc output voltage are equal to the switch voltage and diode voltage. The inductor current will be freewheeling inside the input side itself. This mode ends with the start of the next switching cycle. The time period of this mode is calculated by

$$\Delta_1 = \frac{V_{ac}}{V_{dc}} \times d \quad \rightarrow \quad (7)$$

Where d is the duty cycle

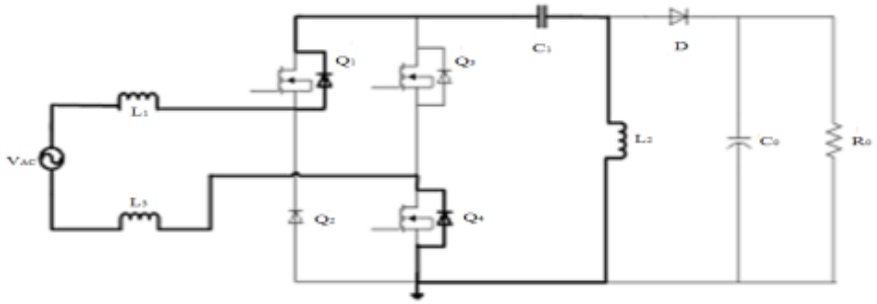

Fig 2.5: Conduction mode 3 of the bridgeless SEPIC converter

III. DESIGN OF PROPOSED CONVERTER

The components used in building up the SEPIC PFC converter [15-17] are input voltage 25 V, frequency 60 HZ, output voltage 10 V_{dc} .The input current ripple should be within 20 % to the peak current of I_{ac}. The switching frequency is said to be 30 kHz. The inductor value L_1, L_2 and L_3 value are computed by the equations below. The efficiency is 95% and following equation is derived

$$I_{ac} = I_{ac\_peak} \sin(\omega t) = \frac{2 \times P_0}{\eta \times V_{ac\_peak}} \sin(\omega t) \quad \rightarrow \quad (8)$$

I_{ac_peak} =140 mA

Input side current ripple

ΔI_L = 20% I_{ac_peak} = 28mA

$$\Delta I_L = \frac{V_S \times d}{L_1 \times f_s} \quad \rightarrow \quad (9)$$

The switching period of the output voltage is obtained by

$$i_{dc\_avg} = 0.5\, i_{dc\_avg}\, \Delta_1 \quad \rightarrow \quad (10)$$

where, i_{dc_avg} is the peak voltage of diode D , Δ_1 is the duty ratio and i_{dc_avg} can be calculated by

$$i_{dc\_avg} = i_{L1} + i_{L2} = \left(\frac{1}{L_{1,s}} + \frac{1}{L_2}\right) V_{ac}\, dTs \quad \rightarrow \quad (11)$$

$$i_{dc\_avg} = 0.5 \left(\frac{V_{dc}^2}{\left(\frac{1}{L_{1,s}} + \frac{1}{L_2}\right) V_{dc}} d^2 T_s \right) \quad \rightarrow \quad (12)$$

$$i_{dc\_avg} = (1/\pi) \int_0^{\pi} i_{dc\_avg}\, d\,\omega t = \frac{V_{ac\_peak}^2}{4 L_e V_{dc}} d^2 T_s \quad \rightarrow \quad (13)$$

The duty cycle is calculated by

$$d = \frac{V_{dc}}{V_{ac} + V_{dc}} = 0.22 \quad \rightarrow \quad (14)$$

The inductor L_e is calculated by

$$L_e = \frac{V_{ac\_peak}^2 \times d^2}{4 \times V_{dc} \times f_s \times i_{dc\_avg}} = 180\ \mu H \quad \rightarrow \quad (15)$$

The value of L_1 and L_3 are calculated

$$L_{1,3} = \frac{V_{ac\_peak} \times d}{f_s \times \Delta I_L} = 8.8 \text{ mH} \quad \rightarrow (16)$$

$L_1 = L_3 = L_{1,3} / 2 = 4.4$ mH

Then L_2 is obtained from below equation

$$\frac{1}{L_2} = \frac{1}{Le} - \frac{1}{L1,3} \quad \rightarrow (17)$$

$L_2 = 100$ µH

The output capacitance value is calculated by

$$C_0 = \frac{P_{load}}{V_{dc} \times \Delta V_{dc} \ (\%) \times 4 \times f_{ac}} = 2.2\,mF \quad \rightarrow (18)$$

The multi loop fashion is proposed for the SEPIC converter. This is done to generate the reference current to regulate the DC output voltage through the PI controller. This makes the outer voltage controller loop. The gate pulse to the switches is generated by the inner controller loop through PI controller. The output DC voltage is passed through a band stop filter where it will filter switching ripples and the noise in the DC output voltage.

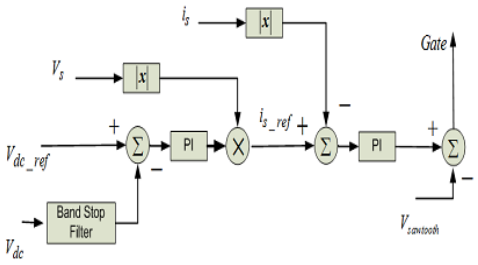

Fig 3.1: Power factor correction controller

IV. SIMULATION RESULT

The simulation result of conventional SEPIC and bridgeless SEPIC is discussed in order to project the difference between them. And this presents the result of input voltage, output voltage, input current, output current, power, power factor and Total Harmonics Distortion analysis.

Table 4.1: Simulation Parameter

PARAMETER	**CONVENTIONAL SEPIC**	**PROPOSED SEPIC**
F_{SW}	30KHZ	30KHZ
L	100µH 4.4Mh	100µH 4.4mH, 4. 4Mh
C	2200µH	2200µH
R LOAD	40 ↄ	40 ↄ
PI	$K_{P=}$0.1 $K_{I=}$ 1	$K_{P=}$0.1 $K_{I=}$ 0.75

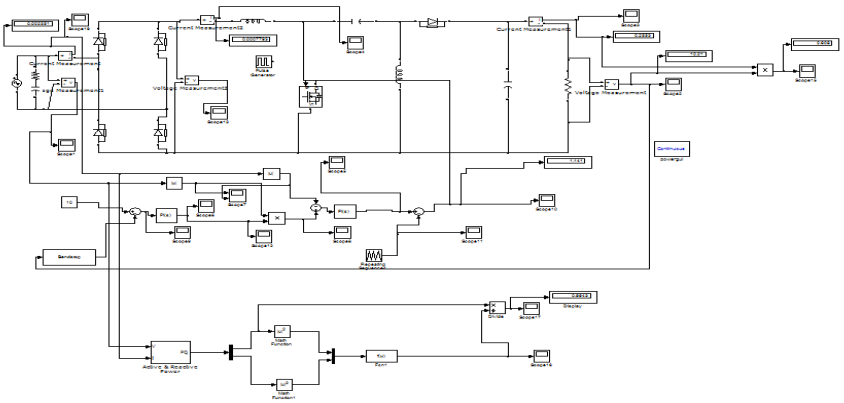

Fig 4.1: Simulated diagram of conventional SEPIC PFC converter

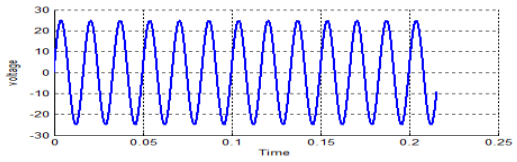

Fig 4.2: Voltage waveform for conventional SEPIC PFC converter

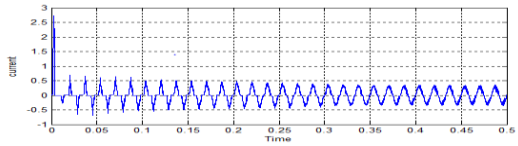

Fig 4.3: Current waveform for conventional SEPIC PFC converter

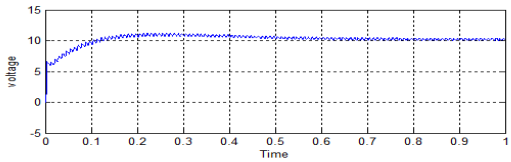

Fig4.4: Output voltage waveform conventional SEPIC PFC converter

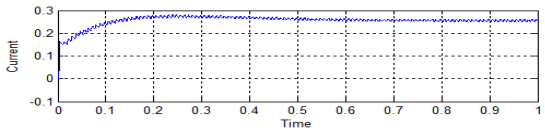

Fig4.5: Output current waveform conventional SEPIC PFC converter

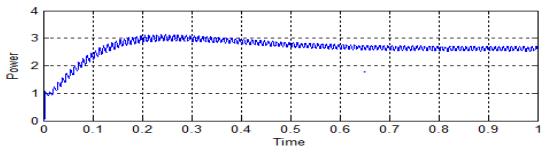

Fig4.6: Output power waveform for conventional SEPIC PFC converter

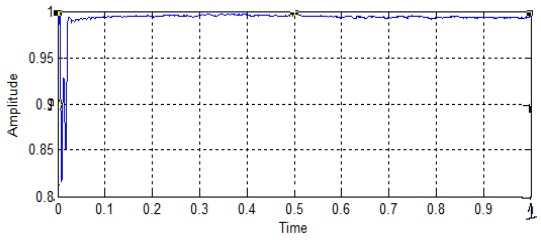

Fig 4.7: Power factor curve for conventional SEPIC PFC converter

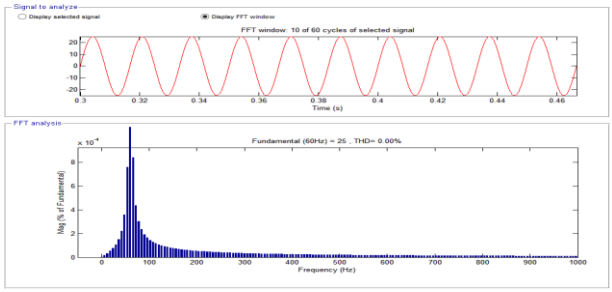

Fig 4.8: THD analysis of the input voltage for conventional SEPIC PFC converter

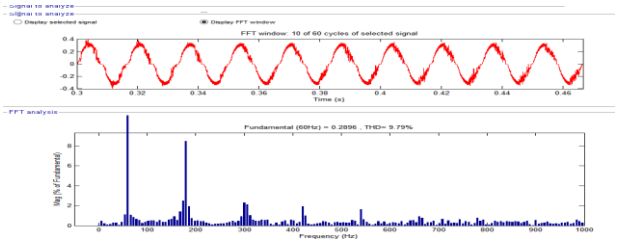

Fig4.9: THD analysis of input current for conventional SEPIC PFC converter

The bridgeless SEPIC converter result is presented in order to show the better result than the conventional SEPIC converter.

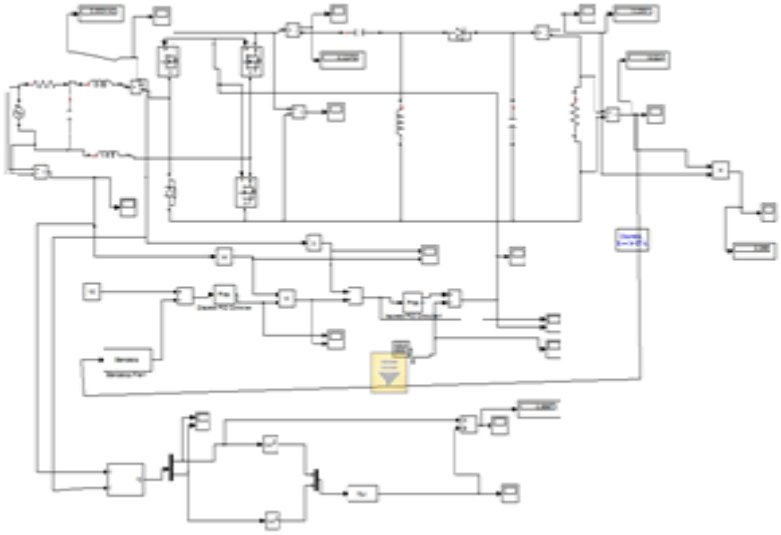

Fig4.10: Simulated diagram of bridgeless SEPIC PFC converter

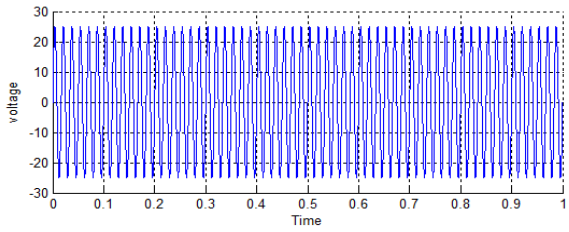

Fig4.11: Input current waveform for bridgeless SEPIC PFC converter

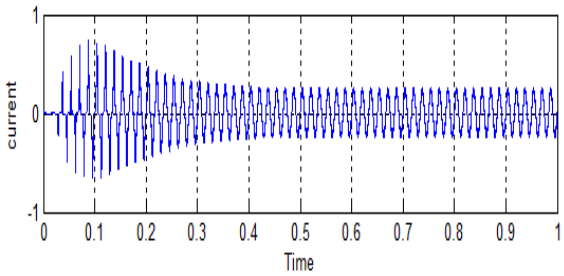

Fig4.12: Input current waveform for bridgeless SEPIC PFC converter

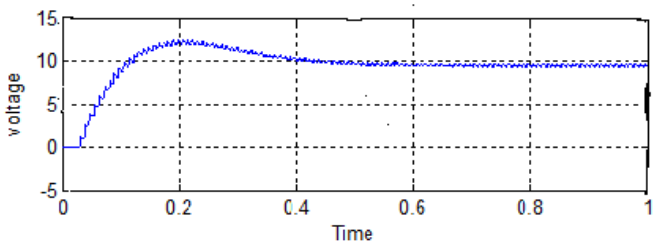

Fig4.13: Output voltage waveform for bridgeless SEPIC PFC converter

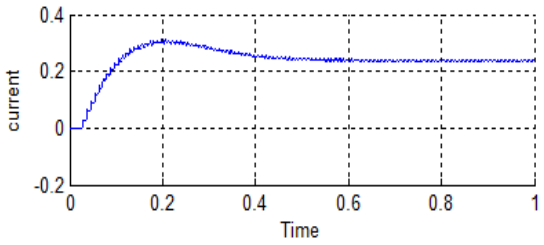

Fig4.14: Output current waveform for bridgeless SEPIC PFC converter

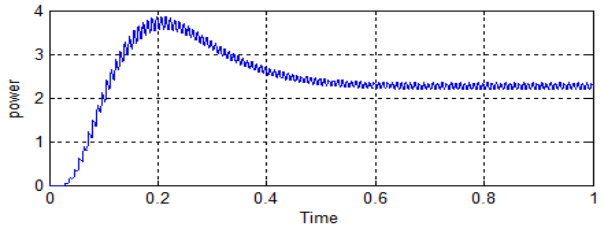

Fig4.15: Output power waveform for bridgeless SEPIC PFC converter

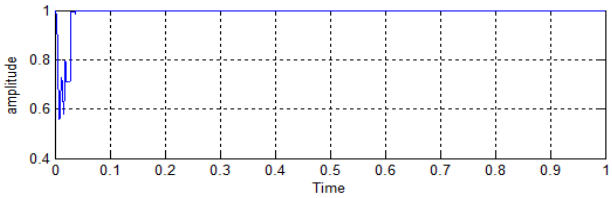

Fig4.16: Power factor curve for bridgeless SEPIC PFC converter

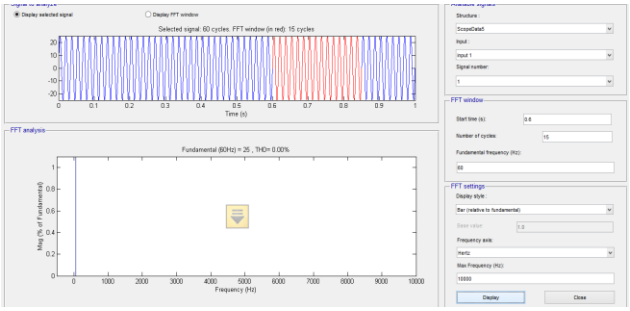

Fig4.17: THD of the input voltage for bridgeless SEPIC PFC converter

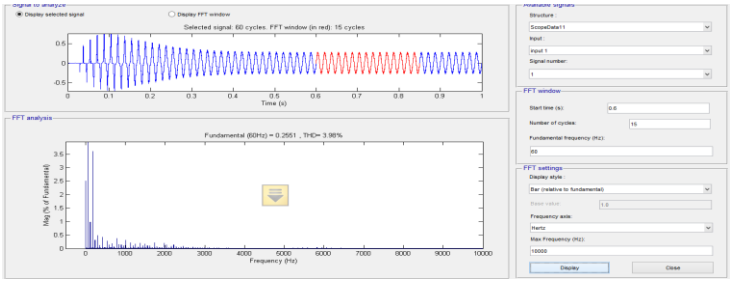

Fig4.18: THD of the input current for bridgeless SEPIC PFC converter

Table4. 2: Comparison study of conventional SEPIC and proposed SEPIC PFC converter

	THD	PF
Conventional SEPIC PFC converter	9.37	0. 994
Proposed SEPIC PFC converter	3.98	0.999

V. HARDWARE RESULT

The experimental circuit of the proposed converter is developed for the design provided in it. The experimental setup is provided below

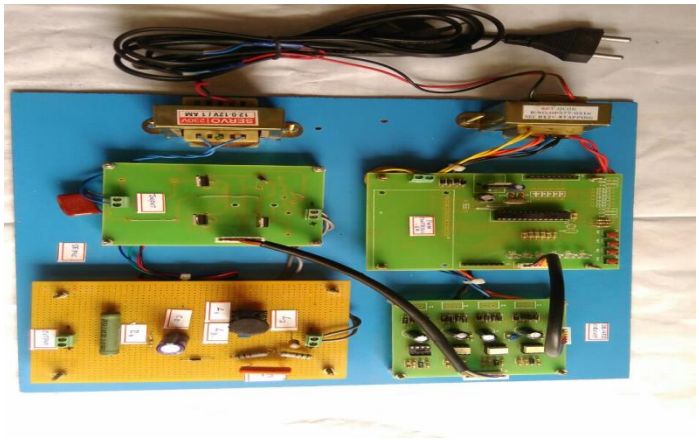

Fig 5.1: Total setup of DSPIC2010

The DSPIC2010 MC consists of 28 pins in that 1st pin for the supply .The 28 pin in the ground. The pulse output is generated in 23 to27 pins. Input inductors L1, L3 and output inductor L2 are chosen as per design value for diodes are selected. The control circuit is implemented using the digital signal processing DSP1C2010 MC. The experimental results of input voltage, input current and output voltage for conventional SEPIC PFC are shown in the simulation. For the input voltage of 25 V, output voltage of 10 V, and the input current of 140 mA, the THD is measured to be 9.37%, with a power factor of 0.994. The experimental results of input voltage, input current and output voltage for the proposed SEPIC PFC are shown in Fig. 12 and13. For the input voltage of 25 V, output voltage of 10 V, and the input current of 136 mA, the THD is measured to be 2.837%, with a power factor of 0.998. The output voltage ripple is obtained 0.15 V at 10 V_{DC} as it is shown in Fig. 13. The phase of the input current is similar to the input voltage and the obtained PF is near unity.

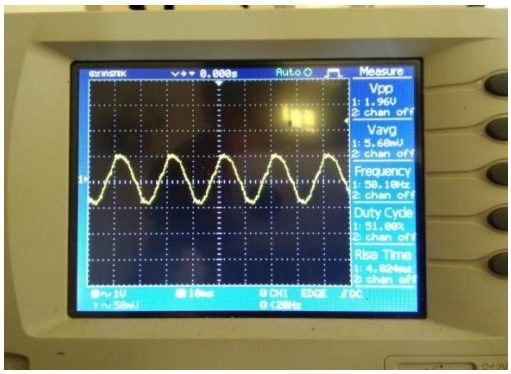

Fig 5.2 Input voltage of the bridgeless SEPIC converter

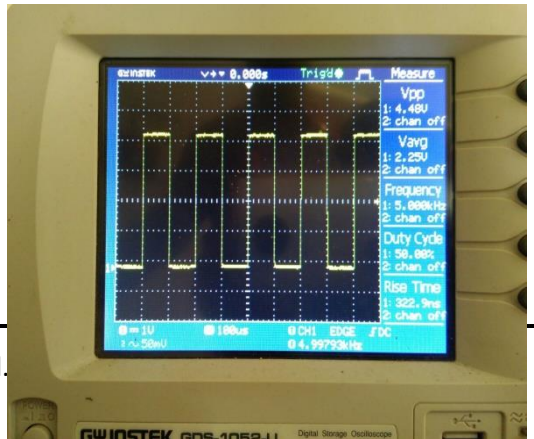

Fig 5.3: Pulse for MOSFET of the bridgeless SEPIC converter

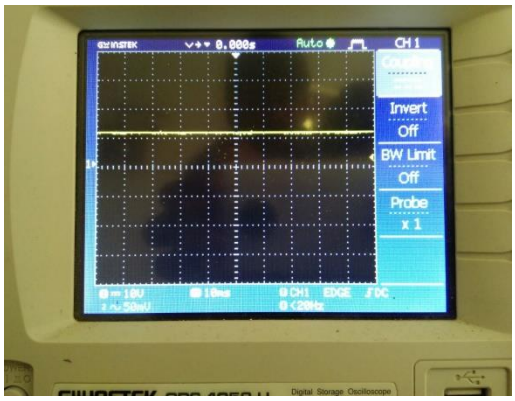

Fig 5.4: Output voltage waveform for bridgeless SEPIC converter

V1. CONCLUSION

This paper presents conventional SEPIC converter and bridgeless SEPIC converter. The basic conflict between them is input full bridge rectifier. And this is executed to improve PF and reduces the THD in the utility grid. Analysis of two converters is done and the yields are displayed. The power factor of conventional SEPIC converter is 0.994% and THD is 9.37%. The power factor of the proposed SEPIC converter is 0.999% and THD is 3.98%. The proposed SEPIC converter is used for low power application with high quality input.

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