DEVELOPMENT OF HIGH RESILIENCY FEEDBACK CONTROLLERS FOR POSITIVE OUTPUT ELEMENTARY SUPER LIFT LUO CONVERTER

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Abstract: The Positive Output Elementary Super Lift Luo Converter (POESLLC) is the most topical topology of DC-DC converter family. It has higher voltage transfer gain, good efficiency, and diminished inductor coil current and capacitor voltage ripples. The controller of POESLLC must handle with their inherent nonlinearity and broad input voltage and load variations, guarantying stability in any operating condition while providing fast transient and enhanced dynamic responses. The conquest of non-linear controller lies in performing superior against these problems of the variable structure system (VSS), that is as DC-DC converter. This paper rekindles the working of POESLLC, first and develops two feedback controllers, proportional-integral controller (PIC) and fuzzy logic controller (FLC), secondly. The designed POESLLC and developed controllers are schematized in MATLAB-Simulink. The simulation study is performed in MATLAB/Simulink software with ODE Solver ode23tb.

Keywords- *Positive Output Elementary Super Lift Luo Converter (POESLLC), Fuzzy logic controller (FLC), Proportional integral controller (PIC), Voltage ripple*

I. INTRODUCTION

DC-DC converters have their ascendancy in many vital applications as power supplies, namely, the industries like telecommunication, medical, defense, computing, aerospace etc. Basically, the DC-DC converters are of two types; the buck converter that reduces the voltage level from an input DC source and the boost converter that increases the voltage level of the input source [1]. Switch mode DC-DC power converters are employed in order to transform an unregulated DC voltage input (i.e. a voltage that possibly contains disturbances) in a regulated output voltage. For example, a DC-DC power converter can transform an unregulated (i.e. distorted) 12V input voltage in a regulated (i.e. clean) voltage of 36V at the output. Some DC-DC power converters have a fixed output reference and ensure that such voltage is always delivered, no matter what the input is; some others can have a variable output reference, which can be therefore set depending on the current need of the device the power converter is used in. The converter system to be discussed in this project belongs to this first category [2]-[5]. This leads to the

requirement of more advanced control methods to meet the demand. Few such control methods have been developed to control a contemporary family of DC-DC converters.

In recent days, the DC-DC conversion topologies experiences an unparalleled growth and are becoming increasingly common in applications such as medical equipment, telecommunication network, computer systems, industrial production lines, defense electronic power supplies, renewable energy power systems, military applications and many more. Today more than 500 topologies of DC-DC converters have been archived. The topological evaluation in this field includes the development of converters such as the buck, boost, buck–boost, Cuk, single-ended primary inductor converter (SEPIC), Zeta converter, isolated converters, Luo family converters, KY converter etc., where the primary objective is attaining a high voltage transfer gain [6]-[10]. The demand of most of the applications is being superior output voltage regulation under the line and load variations as well as the circuit parameters uncertainties, and became the focus of recent researchers.

The analysis and design of a single phase power factor correction (PFC) scheme using a DC-DC single ended primary inductance converter with genetic algorithm (GA)-tuned proportional integral controllers (PIC) have been provided [11]. A systematic off-line design approach using GA for optimising the parameters of the PI controller has been proposed and the performance has been compared with the conventional Z-N tuned PI controller. The steady-state and transient responses of the converter subjected to a change in the load, set point and line variations have been examined. The development of an improved output feedback controller for the positive output super-lift re-lift Luo converter has been coined [12].

The main feature of the proposed controller is that even though the non-minimum phase obstacle presented by the boost-type dc-dc converter, the output voltage is regulated directly. Moreover, the structure of the proposed controller is such that it is insensitive to the load variations and there is no risk of saturation in the control law due to division by zero. The comparative study of dual-loop current-mode controllers to accomplish the output voltage regulation of the positive output elementary Luo (POEL) converter has been done [13]. The POEL converter is a fourth-order dc-dc boost converter developed using the voltage lift technique that gives a positive load voltage. Two current-mode controllers, one using the input inductor current and one using the output inductor current, are studied. Both state-space and frequency response approaches are used in the study to obtain a better insight of the comparative study. It is established that the controller using the input inductor current is more suitable for the regulation of the POEL converter.

The earlier attempts of developing feedback controllers has considered only the line and load regulations. The perturbations due to parameter variations have not been subsumed. This paper rekindles the working of positive output elementary super lift Luo converter (POESLLC), first and develops two feedback controllers, proportional-integral controller (PIC) and fuzzy logic controller (FLC). The designed POESLLC and developed controllers are schematized in MATLAB-Simulink. The simulation study is performed in MATLAB/Simulink software with ODE

Solver ode23tb. The controller of POESLLC cope with the line voltage variation, change in load and also the circuit parameter variations while providing fast transient and improved dynamic responses.

II. POSITIVE OUTPUT ELEMENTARY SUPER LIFT LUO CONVERTER

Contemporary industrial applications necessitate immense boost-up voltage gains in DC-DC converters. In present days it is very hard to interface applications such as battery backed uninterruptible power supply (UPS), photovoltaic (PV) energy conversion system, fuel cell, medical equipments, robot systems, renewable energy systems etc. The traditional DC-DC converters such as the buck, boost, buck–boost, Cuk, single-ended primary inductor converter (SEPIC), Zeta converter, K-Y converter and Luo family converters fail to offer the voltage transfer gain projected in theoretical calculations due to the upshot of power semiconductor switches, rectifier power diodes, and the equivalent series resistance (ESR) of inductors and capacitors [14]-[18]. Positive output elementary super lift Luo converter (POESLLC) is a one the imperative DC-DC converter topology that gives a positive controlled output DC voltage from a positive DC input voltage. The prime connotation of this converter is higher voltage transfer gain (in geometric progression), excellent efficiency, suppressed inductor current/capacitor voltage ripples. For all portable applications (digital camera, lap-top computers, computer mother board, mobiles etc.), it is mandatory to expand the autonomy of the battery and hence the efficiency is critical even this converter operates at light load or no load conditions.

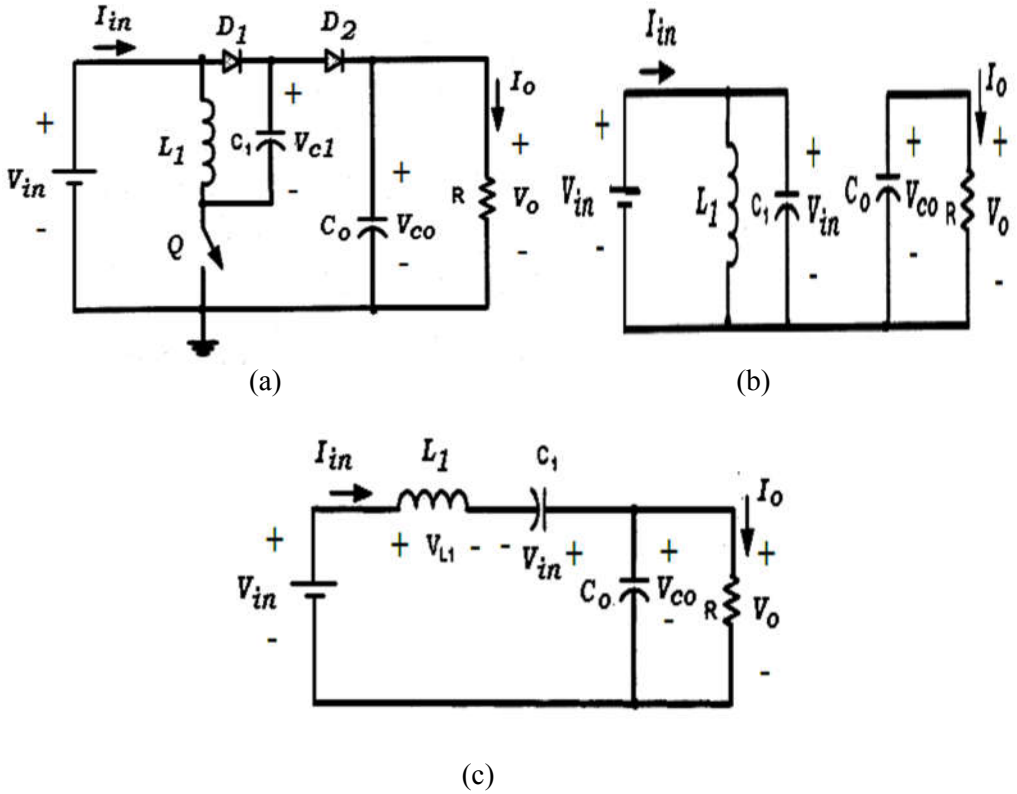


Figure.1. POESLLC (a) Power circuit, (b) mode 1, and (c) mode 2

The power circuit of the POESLLC is pictured in Figure.1(a). The efficient voltage step-up capability can be accomplished by controlling the power switch *Q* of the POESLLC. In the power circuit, V_{in} is a dc input supply voltage, Q is the power switch (n-channel MOSFET) and (D_1, D_2) are freewheeling diodes. Energy storage elements are capacitors (C_1, C_o) and inductor L_1. V_O is the output voltage and R is the load resistance. It is assumed that all the components are ideal and also the POESLLC operates in CCM. To analyze the operation of the POESLLC, the circuit can be divided in to two states, viz. the switch-closed and the switch-open. Figure1 (b) and Figure.1(c) show the two states of operation of the POESLLC.

The mandatory requirements of any power conversion systems are reduced components, smaller size, lower weight, lower cost, higher efficiency, higher reliability, lower switching stresses, wide conversion range, improved supply and load side performances etc. The field driven performance requirements such as the larger voltage gain, huge power density, and decreased ripples in load voltage and inductor current imposed converter topologies and screwed the research direction. In the open loop system, the structure and the switching strategies contribute to achieve the objectives. In the closed loop systems the feedback controller has to take the responsibility. Figure.2 represents a typical feedback structure of POESLLC where the controller can be any one amid PIC, FLC, etc.

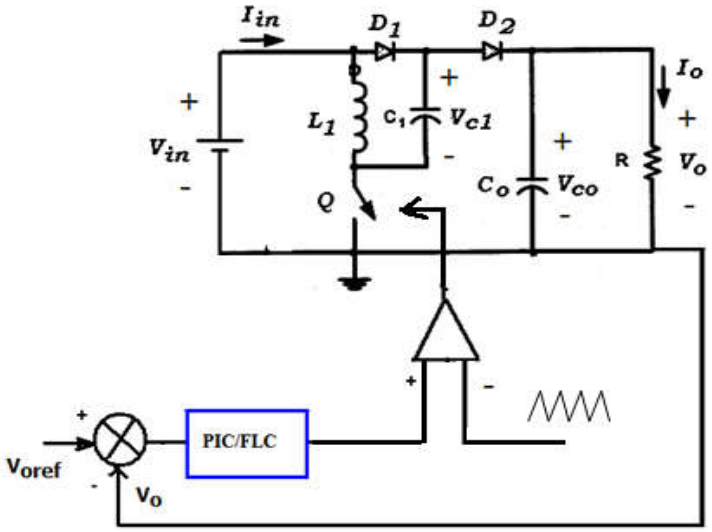


Figure.2 POESLLC with the feedback control structure and controllers

III. DEVELOPMENT OF FUZZY LOGIC CONTROLLER

In this study, the FLC is used to regulate the power switches of the POESLLC operates in continuous conduction mode (CCM). The FLC's fuzzy interference systems (FIS) with assigned inputs and output is shown in Figure.3 (MATLAB). The output voltage error (e) and its change in voltage error (de) of POESLLC is applied as a input the FLC and the output is o (mark the reference current for the inductor). For suitability, the arithmetic ranges of the inputs/output of the FLC can be normalized and expressed as pursues: e = [-0.1 -0.062 -0.036 0 0.036 0.062 0.1],

ce = [-0.2 -0.14 -0.06 0 0.06 0.14 0.2] and o = [-0.1 -0.06556 -0.03334 0 0.03334 0.06556 0.1] and its related fuzzy sets are [NB, NM, NS, Z, PS, PM, PB] where, NB (negative big), NM (negative medium), NS (negative small), Z (zero), PS (positive small), PM (positive medium), PB (positive big), respectively. The membership functions of the error (e), change in error (ce), and output (o) are marked in Figure.4 to Figure.6. The assortment of FLC rules is completely depends on the performance characteristics of the POESLLC. In this study, 49 rules are structured (refer the Table 1). Subsequently, the weighted average method (defuzzification-method) is utilized to complete the fuzzy design. The rule viewer and surface viewer outputs are pictured respectively in Figure.7 and Figure.8 respectively.

Table 1 Developed Fuzzy Rule

E / ce	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	Z
NM	NB	NB	NM	NM	NS	Z	PS
NS	NB	NM	NS	NS	Z	PS	PM
Z	NB	NM	NM	Z	PS	PM	PB
PS	NM	NS	Z	PS	PS	PM	PB
PM	NS	Z	PS	PM	PM	PM	PB
PB	Z	PS	PM	PB	PM	PB	PB

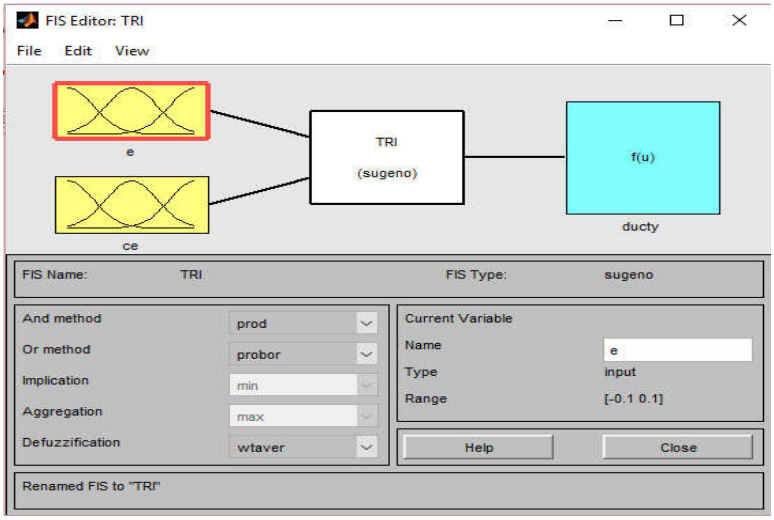


Figure.3 Fuzzy inputs

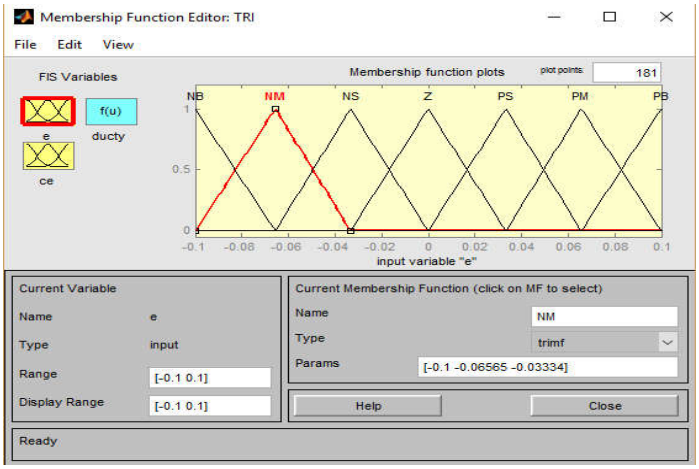


Figure. 4 Membership function for input 1

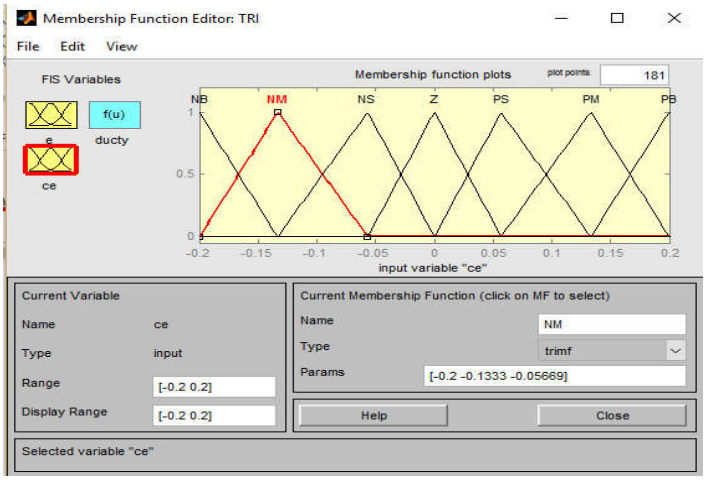


Figure.5 Membership function for input 2

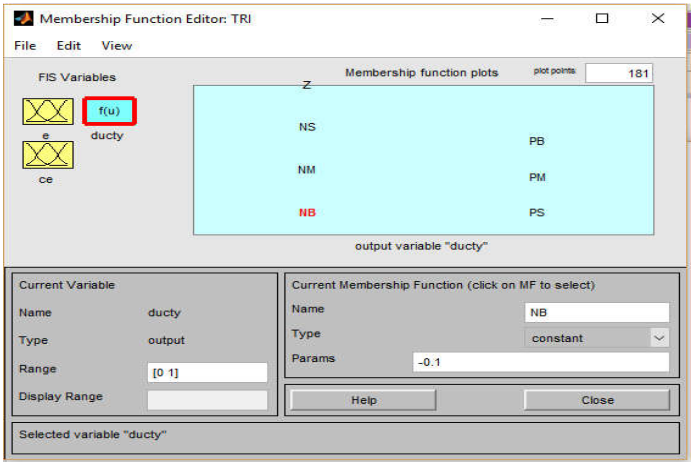


Figure.6 Output variable

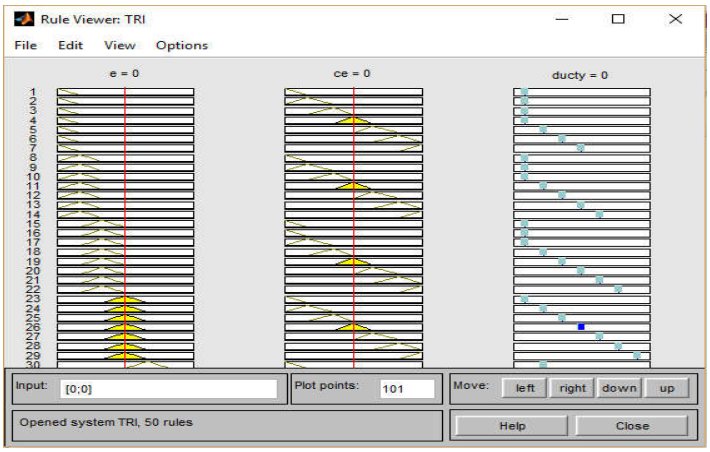


Figure.7 Rule viewer

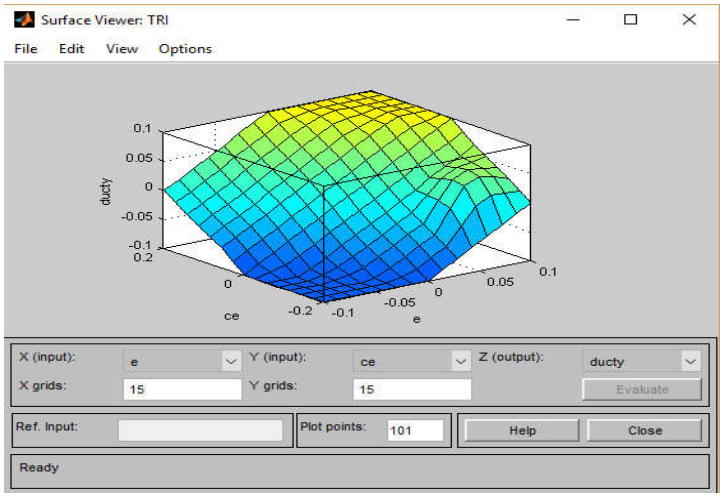


Figure.8 Surface view

IV. RESULTS & DICUSSION

This section deals about the simulation results of POESLLC in CCM using PIC and FLC. The POESLLC in CCM performance is verified at various conditions viz. start-up transient, line variation, load variation, and also circuit components variations. The MATLAB/SIMULINK simulation model of the POESLLC is schematized in CCM with specifications listed in Table 2.

Table 2 Specifications of the POESLLC

Parameters name	Symbol	Value
Input Voltage	V_{in}	12V
Output Voltage	V_o	36V
Inductor	L_1	44.6µH
Capacitor	C_1, C_0	4.7 µF and 22 µF
Nominal switching frequency	F	20kHz
Load resistance	R	416.6Ω
Average input current	I_{in}	0.269A
Efficiency	η	96.48%
Average output current	I_o	0.08641A
Duty ratio	D	0.5
Peak to Peak Inductor Current Ripple	Δ_{iL1}	25% of I_{in}
Peak to Peak Output Capacitor Ripple Voltage	ΔV_o	0.12V

4.1 Start-up Region

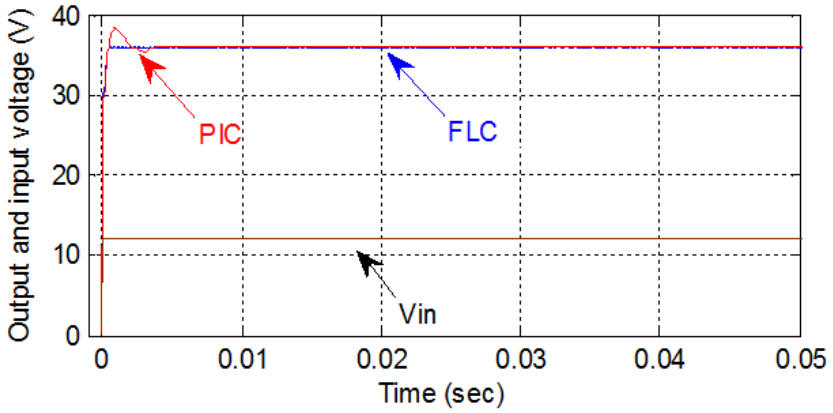


Figure.9 Simulated output voltage responses of POESLLC with rated input voltage (12V)

Figure.9 shows the simulated output voltage results of POESLLC using the PIC and FLC in start-up transient region with nominal input voltage. From these figureure, it is evident that the output voltage of the POESLLC has null overshoots, settling time of 0.0005 s using FLC, but the same converter with PIC has produced peak overshoots of null and settling time of 0.0006s during start-up transient region. Table 3 formulaically compares

the time domain specifications (TDSs) of two cases.

Table 3 Time domain specification during start up

Time Domain Specification	PIC	FLC
Delay Time	0.00071	0.0001
Rise Time	0.00086	0.0002
Peak Time	0.0009	0.0003
Settling Time	0.006	0.0005
Peak overshoot	2.3V	-

4.2 **Line Variation**

The response of output voltage for input step change from 12V to 15 V at time of 0.025s with R = 416.6Ω is provided in Figure.10. The corresponding TDS are tabulated in Table 4. The same kind of study for input step change from 12V to 9 V is also performed and detailed in Figure.11 and Table 5. The corroborated disturbance rejection property of developed feedback FLC is well evidenced**.**

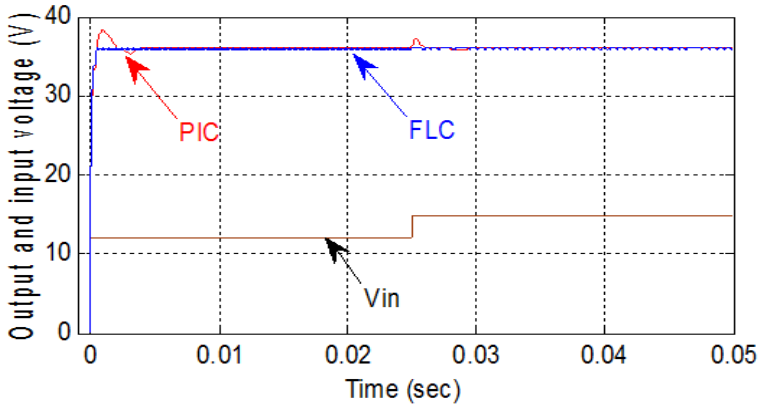
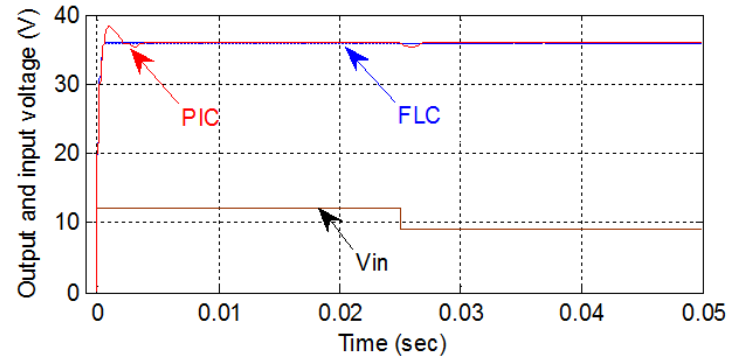


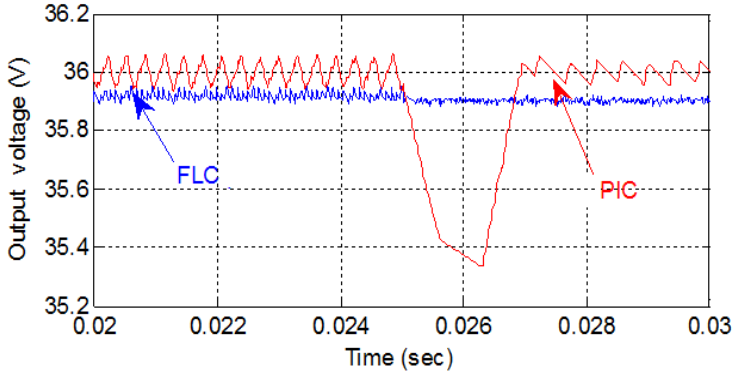
Figure.10. Response of output voltage for input step change from 12V to 15 V at time of 0.025s with R = 416.6Ω

Table 4 Time domain specification during line disturbance 12V to 15V

Time Domain Specification	PIC	FLC
Delay Time	0.00084	0.0002
Rise Time	0.0009	0.00039
Peak Time	0.00095	0.00041
Settling Time	0.007	0.00052
Peak overshoot	2.35V	-



(a)



(b)

Figure.11. Response of output voltage for input step change from 12V to 9 V at time of 0.025s with R = 416.6Ω, (a) Normal view, (b) Enlarged view

Table 5 Time domain specification during line disturbance 12V to 9V

Time Domain Specification	PIC	FLC
Delay Time	0.00068	0.00025
Rise Time	0.00079	0.00031
Peak Time	0.00085	0.00035
Settling Time	0.0068	0.00049
Peak overshoot	2.35V	-

4.3 Load Variation

Both the step increase and decrease disturbances in load (Load change 416.6Ω to 516.6 Ω and 516.6 Ω to

416.6Ω) are studied. The responses are given in Figure.12 and Figure.13 as well as in Table 6 and Table 7.

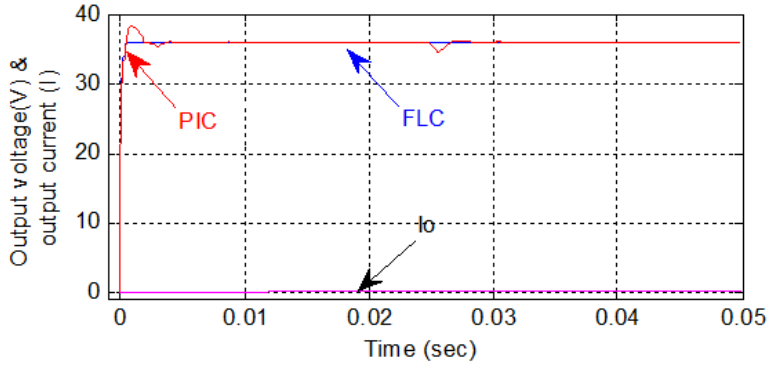


Figure.12. Response of output voltage for Load change 416.6Ω to 516.6 Ω at time of 0.025s with R = 416.6

Table 6 TDS during load disturbance from 416.6Ω to 516.6 Ω

Time Domain Specification	PIC	FLC
Delay Time	0.00045	0.0003
Rise Time	0.00062	0.00042
Peak Time	0.00056	0.00045
Settling Time	0.0063	0.00023
Peak overshoot	2.29V	-

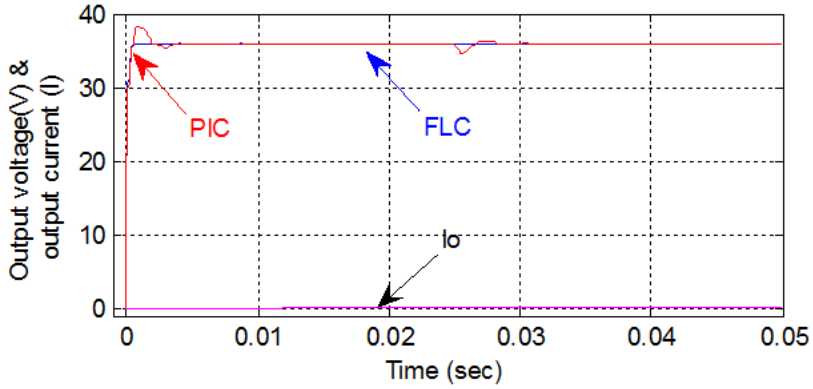


Figure.13. Response of output voltage for Load change from 416.6 Ω to 316.6 Ω at time of 0.025s with R = 416.6Ω

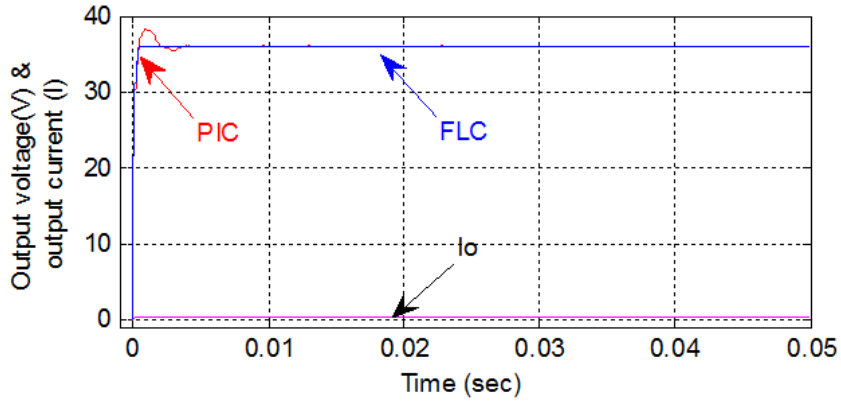
Table 7 TDS during load disturbance from 416.6 Ω to 316.6 Ω

Time Domain Specification	PIC plus SMC	FLC plus SMC.
Delay Time	0.000395	0.00026
Rise Time	0.00048	0.00039
Peak Time	0.00056	0.00044
Settling Time	0.007	0.00058

Peak overshoot	2.4V	-

4.4 Circuit Components variations

The response of output voltage for the component (inductor) change 44.6mH to 90mH at time of 0.025s with R = 416.6Ω, is shown in Figure.14 and Table 8.



(a)

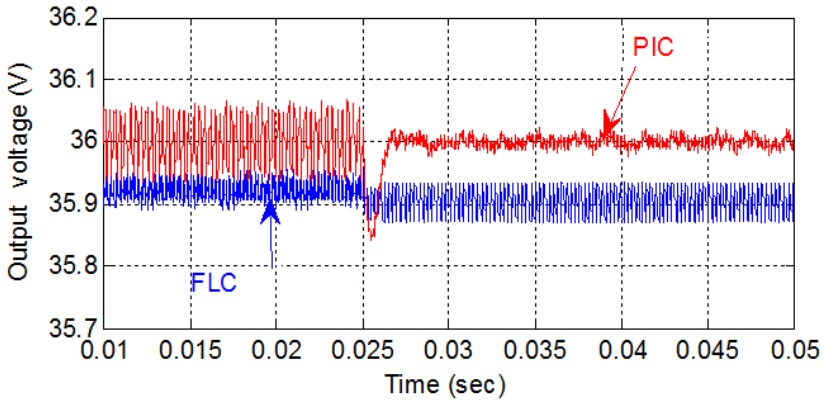


Figure.14. Response of output voltage for component (inductor) change 44.6mH to 90mH at time of 0.025s with R = 416.6Ω, (a) Output voltage and output current (b) Enlarged view of output voltage

V. CONCLUSION

For high power level applications, the CCM boost-type converters are the favored due to their lower conduction loss, reduced current and voltage ripples, and higher voltage gain. But, the major issues with these converters is the voltage regulation against line, load and circuit parameter perturbations. In this article the analysis, design and implementation of high performance POESLLC is discussed in CCM. Also, the paper suggested two feedback controllers viz. PIC and FLC. The developed controllers have been implemented both in MATLAB-Simulink. The merits of developed FLC the PIC are robust to huge changes on line, and load, eliminates the steady state error, easy implementation, and superior quality output response even though the circuit parameter modifications.

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