EIGHTEEN LEVEL ASYMMETRICAL SINGLE PHASE MULTI LEVEL INVERTER TOPOLOGY WITH LOW SWITCHING FREQUENCY AND LESS DEVICE COUNTS

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Abstract- An eighteen level asymmetrical single phase multi-level inverter topology with low switching frequency and less device counts have been proposed in this paper. In this new topology the desired output voltage of the inverter has been obtained by simple combination of addition and subtraction of all DC sources through different switches. The desired output voltage obtained by this method shows that the less number of sources, switch counts, and considerable reduction in losses, cost and size of the inverter. While comparing the proposed topology with the existing one the results shows that the proposed topology needs very less device count, switch counts and components. Matlab based simulation software have been used to analysis the performance of the proposed topology along with mathematic modelling the output of proposed topology simulation shows that the proposed topology need very less count of switch and also the performance of the circuit is fare better than the other conventional topology available in the market.

Keywords: *Multi Level Inverter; Asymmetrical; Low Frequency Switching; Total Harmonic Distortion (THD)*

I INTRODUCTION

The main concept behind the multi-level inverter is to get high level voltages with the help of using the many DC sources along with the switches in small voltage steps. By doing this the output wave form of the inverter becomes nearly sinusoidal [2]. In case of low level application the conventional topology are better convenient as they are not more complex in circuits and device count. But it is not the case as far as high voltage level is concern, and high voltage levels the multi-level inverter topology with the proposed topology will be far better than the conventional [4]. The power electronics devices used as switches will experience very high voltage stress across them in addition to this the output currents also not pure sinusoidal function if the conventional topologies used for high power and high level applications. To overcome this type of problem the new topology with multi-level inverter are used.

The multilevel topology system not only produces the high voltage level needed by the load but also minimize the voltage stress across the power device. This is why the industries go for multi-level inverterfor high level output [6-10]. The output wave form of multi-level inverter will be more or less very closer to the shape of the sinusoidal wave form. The number of level of the multi-level inverter is related with the number of power electronics switches used in the circuit [14-20]. Increase the number of level will leads to increase the number of switches need to obtain the desired level of voltage output of the multi-level inverter. The formula used to link the number of switches need based on the levels is 2 (n-1) where n is the number of levels. So, if 9 level then the switches needs will be 2 (9-1) =16 and so on. This all are in the case of conventional methods. But in multi-level inverters with the new topology in the research the need of switches with increase level are reduce the number of switches. In the new topology of multi-level inverter

with high level output but reduced no of power switches and reduced component count has been categorized in to two topologies, one is the symmetrical MLI topology and the other one is asymmetrical MLI topology [19-21]. The symmetrical topology is nothing but thetopology where the same values of source have been used whereas in asymmetrical MLI topology unequal sources are grouped together to get high level output [6].

The proposed new MLI topology presented in this paper have the capacity to produce high level voltage output with the reduced switch count. The output voltage will be of 18 levels. Here the available sources and switches are arranged in such a way that the maximum combination of addition and subtraction of the input dc source is achieved. The circuit designed have been exercised in the mat lab Simulink software to check its performance and feasibility so that it can be implemented in real time application. The simulation results were obtained for different load condition. The entire paper has been divided in to different section as follows. The section II is deal with configuration of circuit, switching pulse pattern along with the operation of the proposed topology in different mode. In section III, the elaboratediscussions were made about the comparison between the proposed new topology with the other existing topology. Simulation parameter along with results were discussed in the section IV followed by a conclusion.

II PRESENTED TOPOLOGY

A. Circuit Description: The proposed Multi Level Inverter topology consists of three asymmetrical dc sources namely V1, V2 and V3. The IGBTs are used as switches. The total number of switches in this topology is sixteen. The voltage source V1,V2, and V3 are simultaneously considering independent to each other's and they have ratio of V1:V2:V3 = 1:3. This has been done so that the short circuit of sources will not take places. Simultaneous conduction of switches (S1, S2) (S3, S4) (S5, S6) (S7,S8) (S9,S10) (S11,S12) (Sa1, Sa3) (Sa2, Sa4) must be avoided. The switching pulses for one complete cycle have been shown in figure 1(b) and the switches are operated at low frequency. And also conduction periods were very short except for the bridge switches and hence the losses in this topology are reduced considerably.

B. mode of operation: The positive half cycle of the proposed technology along with different mode of operation have been shown in figure 2. The solid lines in the circuit of the mode of operation is indicates the current path of the mode along with source and load. There are eighteen different modes by which the circuit will operated for the completion of one complete cycle. Nine mode of operation for positive half of cycle and another nine mode of operation for negative half cycle and one more mode of operation for the zero level. Thus, eighteen output voltage we get from eighteen mode of operation. The table shows the different modes for positive and negative along with zero level, switching sequence of switches, current path along with source combination and voltage output. The current path and switching sequence are remaining same for positive and negative as well as zero levels. The switches Sa1 and Sa4 are operated during positive half cycle whereas the switches Sa2 and Sa3 are operated during negative half cycle.

III COMPARISON WITH OTHER TECHNOLOGY

The present proposed topology has been compared with the conventional cascaded H -bridge (CHB), Neutral Point Capacitor (NPC), Fly Capacitor (FC) and other topology list out in [16]. The parameters taken or consider for the comparison of the below methods with this proposed method is switches, diodes, dc links and total number of components count. The below table give the comparison details as discussed above.

Table number 1: Simulation

Switches/ Voltage level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
V1	1	0	0	0	1	0	0	0	1	0	0	0

V2-v1	0	1	1	0	0	1	0	1	1	1	0	0
V2	1	0	1	0	0	1	0	1	1	1	0	0
V1+v2	1	0	0	1	0	1	0	1	1	0	0	0
V3	1	0	1	0	0	0	0	0	0	0	1	1
V1+v3	1	0	0	0	0	0	1	0	0	0	1	0
V3+v2-v1	0	1	1	0	0	1	0	0	0	1	1	0
V2+v3	1	0	1	0	0	1	0	0	0	1	1	0
V1+v2+v3	1	0	0	1	0	1	0	0	0	0	1	0

A. Simulation circuit parameters: In order to verify the performance of the presented topology, simulation based on the fig.1 is developed in the matlab based Simulink software. The Simulink frequency used in this circuit for the purpose of simulation is the fundamental frequency of 50 Hz. There are three DC sources are taken in to consideration and the values of

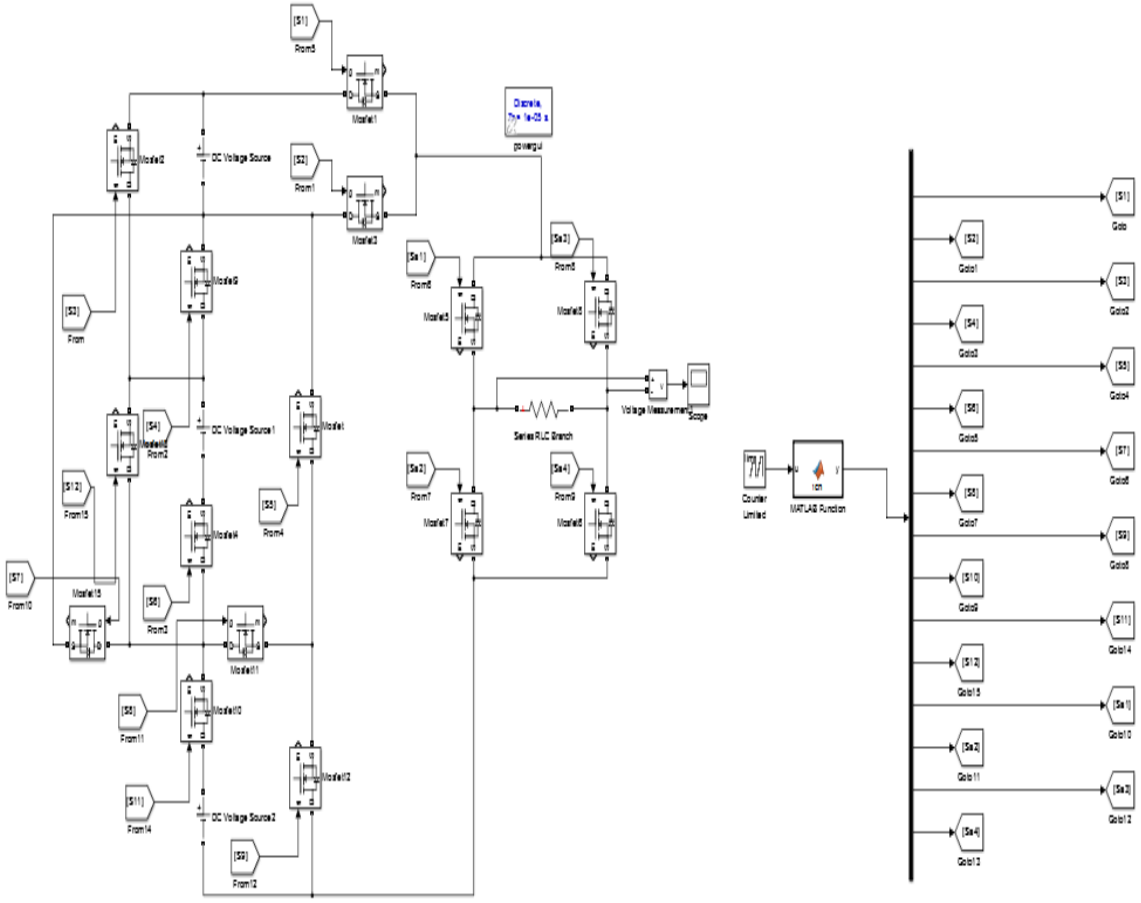

figure.1 is developed in the matlab based Simulink software

each have been set as follows: V1=50V, V2=75 V, V3= 100V. The inverter is operated in open loop mode and different load conditions are assumed. Many control techniques are available in practical but in this system the fundamental frequencyswitching control modulation scheme has been used[1]. The reference signal used here is a sinusoidal voltage wave form which has been compare with the DC sources used in this topology. The switching losses are very low as this topology is low switchingfrequency method.

B. **Simulation result**: The switching pulses given to different switching devices are shown in fig. 2 (a) and (b) for this proposed eighteen level multi-level inverter (MLI) topology. The switches are operated according to the table number 1. By doing this the occurrence of short circuiting the sources are avoided.

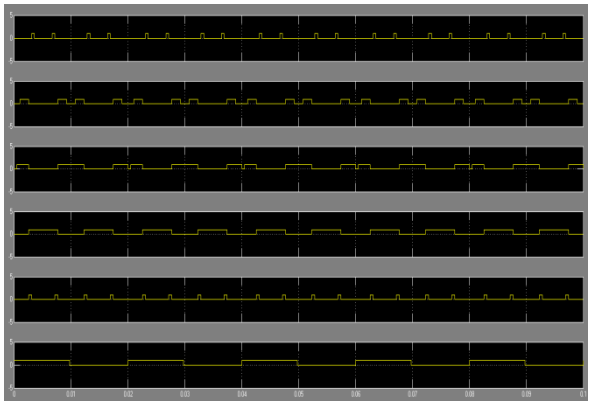

Figure.2 (a) switching pulses

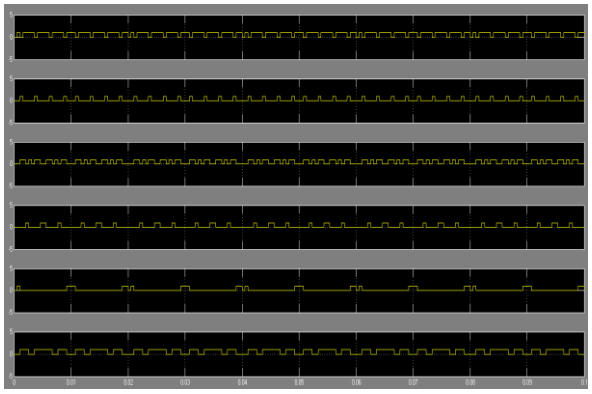

Figure.2 (b) switching pulse

The load used here is of resistive load. The output voltage and current wave form of the inverter and their corresponding harmonic spectrum for the above said load has been shown in the fig. 3(a) & (b). The voltage wave form shows that the proposed topology is able to generate eighteen level output along with almost uniform step size. The output current wave form is shown in fig.3 (c) & (d).

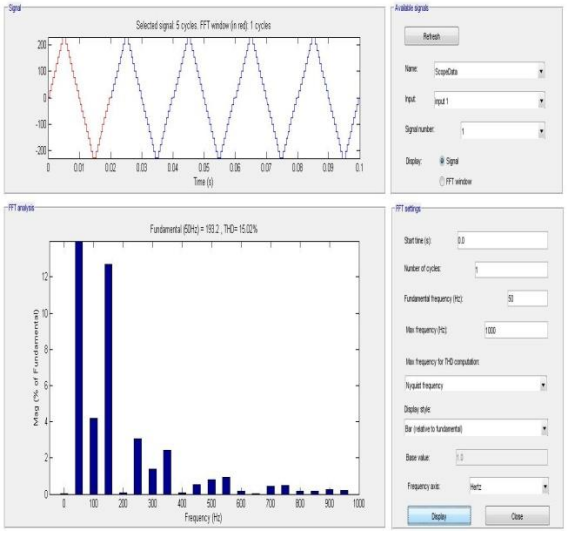

Figure.3 (a) voltage output harmonic spectrum

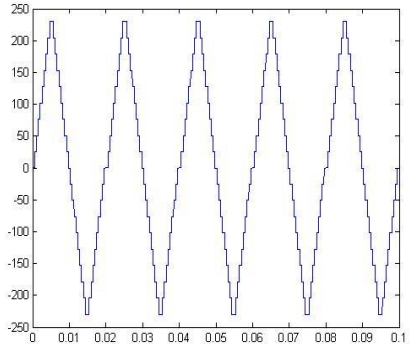

Figure.3 (b) voltage output

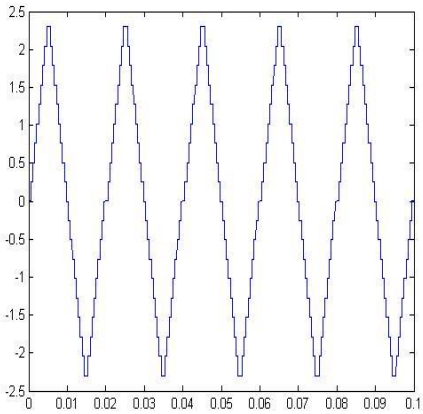

Fig.3 (c) current output wave form

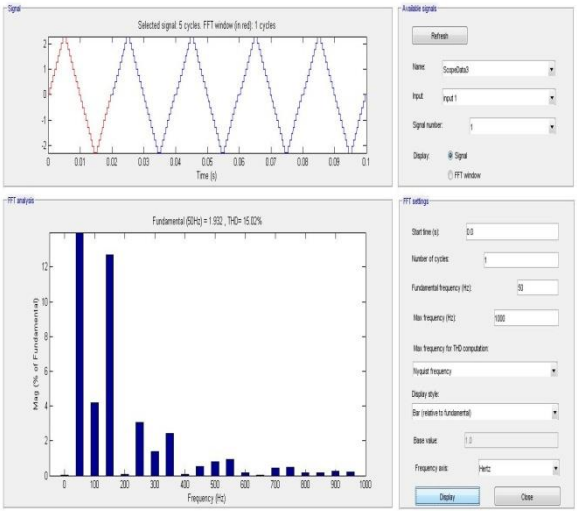

Fig.3 (d) current output harmonic spectrum

This simulation results justify the operation of the presented topology.

The output voltage without using the filter has total harmonic distortion (THD) of 15.2 % and the magnitude of each individual harmonics is less than 5%. This is satisfying the condition of IEEE-519 standard.

IV CONCLUSION

A new single phase eighteen level multi-level inverter (MLI) topology have been presented in this paper. This proposed topology has capacity to produce eighteen level output voltage with reduced device count. This new eighteen level MLI topology can be applied in medium and high power application with

unequal DC sources. The different mode of operation of the inverter topology has been discussed. This proposed topology is compared with other topology of nine level MLI and comparisons shows that this method is far better than other methods as the result is very better. The simulation work is done in the mat lab. Results obtained shows that this topology works out very perfectly. The detailed simulation analysis has been done.

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