FPGA Implementation of Dadda Multiplier Using Approximate 4-2 Compressor

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Abstract-- Importate estimated processing for lower power and less delay for computerized mathematic design. This paper introduce the **"FPGA implementation of Dadda multiplier utilizing approximate 4-2 compressor"** utilized as a part of uses like multimedia and image processing can repulsive mistake and imprecision in calculation and delivered valuable result. The Dadda multiplier was designed by utilizing 4 - 2 compressor which expend less power and less PDP (power delay item) and less delay. FPGA execute of multipliers assume essential part in the configuration of sight and sound and picture preparing center. The design is executed in SPARTAN 3-XCS400 FPGA and asset utilized are 59 cuts 104 LUT, and the delay assessed is 23.419ns with the speed evaluation of – 5.

Keywords- FPGA, Dadda Multiplier, 4-2 compressor, Power delay, 104 LUT, XCS400.

I. INTRODUCTION

Most computerized mathematic applications are executed utilizing digital logic circuits, in this manner working with a high degree of reliability and precision. In any case, numerous applications, for example, in multimedia and image processing can endure mistakes and imprecision in calculation and still produce important and helpful results. Exact and precise models and algorithm are not generally suitable or productive for use in these applications. The paradigm of inaccurate calculation depends on relaxing completely precise and totally deterministic building modules when for instance, planning energy efficient system. This permits uncertain calculation to divert the current design procedure of computerized circuits and systems by exploiting a reduction in multifaceted nature and expense with conceivably a potential increment in execution and force productivity. In exact (or vague) figuring depends on utilizing this property to design disentangled, yet inexact circuits working at higher execution and/or lower power utilization contrasted and exact (definite) logic circuits..

Expansion and multiplication are broadly utilized operations as a part of computerized mathematic; for expansion adders and proposed a few new measurements for assessing rough and probabilistic adders as for brought together figures of legitimacy for outline appraisal for estimated processing applications. For every data to a circuit, the Error Distance(ED) is characterized as the mathematic separation between a mistaken yield and the right one. The Mean Error Distance (MED) and normalized error distance (NED) are proposed by considering the averaging impact of various inputs and the standardization of multiple-bit adders. The NED is almost invariant with the measure of an execution and is accordingly valuable in the unwavering quality evaluation of a particular configuration. The trade-off in the middle of accuracy and force has additionally been quantitatively assessed in.

However, the design of approximate multipliers has gotten less consideration. Multiplication can be thought as the rehashed summation of partial products; however, the clear use of estimated adders when outlining an approximate multiplier is not suitable, on the grounds that it would be extremely wasteful regarding accuracy, equipment many-sided quality and other execution measurements. A few rough multipliers have been proposed in the writing. A large portion of these outlines utilize a truncated multiplication strategy; they evaluate the slightest critical segments of the incomplete items as a consistent. In [4], an uncertain exhibit multiplier is utilized for neural system applications by precluding a portion of the minimum critical bits in the fractional items (and accordingly uprooting a few adders in the cluster). A truncated multiplier with an amendment steady is proposed in. For an n×n multiplier, this outline figures the total of the n+k most critical sections of the incomplete items and truncates the other n-k segments. The n+k bit result is then adjusted to n bits. The reduction error (i.e. the blunder produced by truncating then-k slightest noteworthy bits) and adjusting mistake (i.e. the blunder created by adjusting the outcome to n bits) are found in the following step. The adjustment steady (n+k bits) is chosen to be as close as would be prudent to the assessed estimation of the whole of these errors to reduce the mistake separation.

A truncated multiplier with consistent adjustment has the maximum error if the fractional products in the n-k minimum significant sections are all ones or all zeros. A variable redress truncated multiplier has been proposed in. This technique changes the amendment term in light of segment n-k-1. In the event that every single fractional item in columnn-k-1 are one, then the revision term is expanded. Essentially, if every halfway item in this segment are zero, the remedy term is decreased. In, a streamlined (and therefore mistaken) 2x2 multiplier piece is proposed for building bigger multiplier exhibits. In the configuration of a quick multiplier, compressors have been generally used [8-10] to accelerate the incomplete item lessening tree and diminishing force dissemination. Upgraded plans of 4-2 careful compressors have been proposed in [8, 11 - 16]. [17] [18] have additionally considered pressure for inexact multiplication. An estimated marked multiplier has been proposed for use in arithmetic data value speculation (AVDS); increase is performed utilizing the Baugh-Wooley calculation. In any case, no new design is proposed for the compressors for the estimated calculation. Designs of approximate compressors have been proposed in [18]; however, these plans don't target increase. It ought to be noticed that the methodology of [7] enhances over [17] [18] by using a streamlined multiplier piece that is amiable to approximate multiplication.

In this paper, two novel approximate 4-2 compressors are examine for FPGA implementation. The simplified compressors have preferred delay and power utilization over the streamlined (precise) 4-2 compressor designs found in the specialized literature [8].These approximate compressors are then utilized as a part of the reclamation module of a Dadda multiplier for FPGA execution distinctive plans are proposed for inaccurate multiplication. Broad reproduction results are given at circuit-level to figures of legitimacy, for example, delay, transistor tally, power dissemination, error rate and standardized mistake separation under CMOS highlight sizes of 32, 22 and 16 nm. The use of these multipliers to picture preparing is then introduced. The aftereffects of two samples of increase of two pictures are accounted for; these outcomes demonstrate that the third and fourth inexact multipliers yield a yield item picture that has a high calibre and likeness to the picture created by a precise multiplier, i.e. brilliant qualities for the normal NED and the Peak Signal-to-Noise Ratio (PSNR) are found (for the PSNR more than50db). The investigation and re-enactment results demonstrate that the proposed surmised plans for both the compressor and the multiplier are suitable contender for vague computing. This paper is sorted out as takes after. Area 2 is an audit of existing plans for (precise) compressors. The two new designs of a approximate 4-2 compressor are exhibited in Section 3.Multiplication and two distinctive rough multipliers are proposed in Section 4. Simulation results for the rough compressors and multipliers are given in Section 5.conclusion 6.Results

A broadly utilized structure for pressure is the 4-2 compressor can be actualized with carry bit between nearby slices. The convey bit from the position to the privilege is indicated as cin while the carry bit into the higher position is meant as cout. The two yield bits in positions I and i+1 are likewise alluded as the entirety and carry individually.

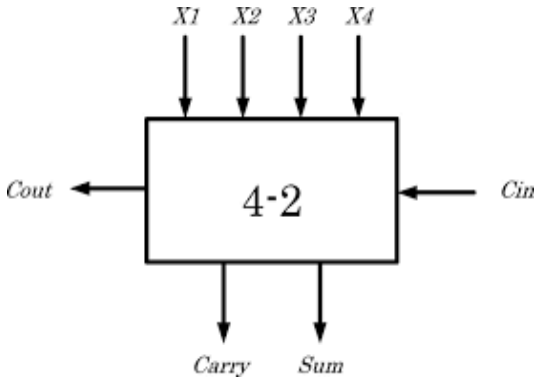


Figure 1.1: Block Diagram Of 4-2 compressor

II. DEFINITE COMPRESSORS

The accompanying mathematical statements give the yields of the 4-2 compressor, while Table 1 demonstrates its truth table.

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin$$
$$Cout = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1$$
$$Carry =$$
$$(x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4$$

The basic usage of a 4-2 compressor is proficient by using two full-adder (FA) cells [8]. Diverse outlines have been proposed in the writing for 4-2 compressor [4, 18, 14, 5, 12, 7, and 3].

Figure1 demonstrates the enhanced design of an exact 4-2 compressor taking into account the purported XOR-XNOR gates [4]; a XOR-XNOR gate at the time all the while creates the XOR and XNOR yield signals. The configuration of [4] comprises of three XOR-XNOR (signified by XOR*) gates, one XOR and two 2-1MUXes. The basic way of this configuration has a postponement of 3δ, where Δ is the unitary deferral through any entryway in the outline.

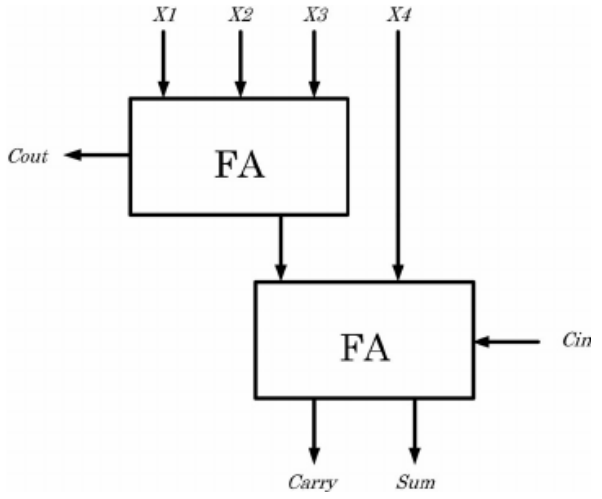


Figure 2.1: 4-2 compressor implementation

2.1.Design 1:

As appeared in Table I, the carry output in a approximate compressor has the same estimation of the information cin in 24 out of 32 states. Along these lines, an inexact configuration must consider this element. In Design 1, the carry is disentangled to cin by changing the estimation of the other 8 outcomes.

Table 1: Truth table of 4-2 compressor

c_{in}	X_4	X_3	X_2	X_1	c_{out}	*carry*	*sum*
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

2.1.1. Carry_1:

Since the Carry outcomes has the higher weight of a binary bit, an incorrect estimation of this sign will deliver a distinction estimation of two in the yield. For instance, if the input design is "01001" (line 10 of Table II), the right outcome is "010" that is equivalent to 2. By rearranging the convey yield to cin, the surmised compressor will create the "000" design at the outcome (i.e. an estimation of 0). This significant distinction may not be satisfactory; in any case, it can be remunerated or decreased by improving the cout and total signs. Specifically, the

$$Carry' = Cin$$

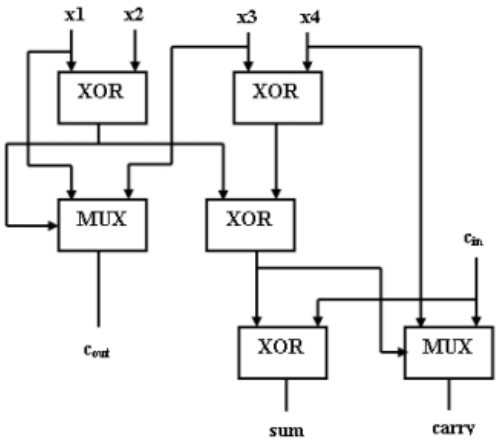


Figure 2.2: Enhanced 4-2 compressor

Rearrangements of whole to an estimation of 0 (second 50% of Table II) lessens the distinction between the rough and the careful yields and in addition the unpredictability of its configuration. Likewise, the vicinity of a few mistakes in the whole flag will brings about a decreases of the postponement of creating the rough total and the general deferral of the configuration (since it is on the basic way).

$$Sum' = \overline{Cin}(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

In the last step, the change of the estimation of cout in a few states, might diminish the mistake separation gave by rough carry and sum furthermore more rearrangements in the proposed design.

$$Cout' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

In spite of the fact that the aforementioned disentanglements of carry and aggregate build the mistake rate in the proposed inexact compressor, its configuration many-sided quality and hence the force utilization are impressively diminished. This can be acknowledged by looking at (2) - (4) and (5)-(7).Table II demonstrates reality table of the initially proposed approximate compressor. It likewise demonstrates the contrast between the vague outcomes of the proposed approximate compressor and the yield of the definite compressor. As appeared in Table II, the proposed plan has 12 mistaken yields out of 32 yields (along these lines yielding a blunder rate of 37.5%).

Table 2: Truth table of first approximate 4-2 compressor

c_{in}	X_4	X_3	X_2	X_1	c_{out}'	carry'	sum'	Difference
0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	0	1	0
0	0	0	1	1	0	0	1	-1
0	0	1	0	0	0	0	1	0
0	0	1	0	1	1	0	0	0
0	0	1	1	0	1	0	0	0
0	0	1	1	1	1	0	1	0
0	1	0	0	0	0	0	1	0
0	1	0	0	1	1	0	0	0
0	1	0	1	0	1	0	0	0
0	1	0	1	1	1	0	1	0
0	1	1	0	0	0	0	1	-1
0	1	1	0	1	1	0	1	0
0	1	1	1	0	1	0	1	0
0	1	1	1	1	1	0	1	-1
1	0	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0	0
1	0	0	1	0	0	1	0	0
1	0	0	1	1	0	1	0	-1
1	0	1	0	0	0	1	0	0
1	0	1	0	1	1	1	0	1
1	0	1	1	0	1	1	0	1
1	0	1	1	1	1	1	0	0
1	1	0	0	0	0	1	0	0
1	1	0	0	1	1	1	0	1
1	1	0	1	0	1	1	0	1
1	1	0	1	1	1	1	0	0
1	1	1	0	0	0	1	0	-1
1	1	1	0	1	1	1	0	0
1	1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0	-1

This is not exactly the mistake rate utilizing the best inexact full-viper cell of [16]. (5)- (7) are the logic expressions for the outputs of the first design of the approximate 4-2 compressor proposed in this manuscript. The gate level structure of the first proposed design shows that the critical path of this compressor has still a delay of 3Δ, so it is the same as for the exact compressor of Figure 5. However, the propagation delay through the gates of this design is lower than the one for the exact compressor. For example, the propagation delay in the XOR* gate that generates both the XOR and XNOR signals in [4], is higher than the delay through a XNOR gate of the proposed design. Therefore, the critical path delay in the proposed design is lower than in the exact design and moreover, the total number of gates in the proposed design is significantly less than that in the optimized exact compressor of [4].

2.2. Design 2:

A second design of a approximate compressor is proposed to further expand execution and also diminishing the mistake rate. Since the carry and cout outcomes have the same weight, the proposed mathematical statements for the estimated convey and cout in the past part can be traded. In this new outline, convey utilizes the right hand side of (7) and cout is constantly equivalent to cin; since cin is zero in the primary stage, cout and cin will be zero in all stages. Thus, cin and cout can be overlooked in the equipment plan. Figure 7shows the square graph of this rough 4-2 compressor and the expressions underneath depict its outcomes.

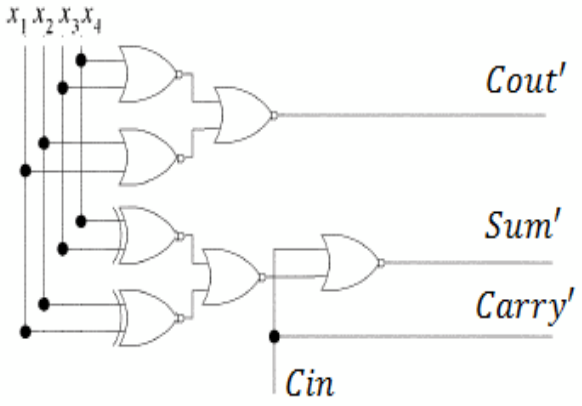


Figure 2.3: Implementation of gate level design1

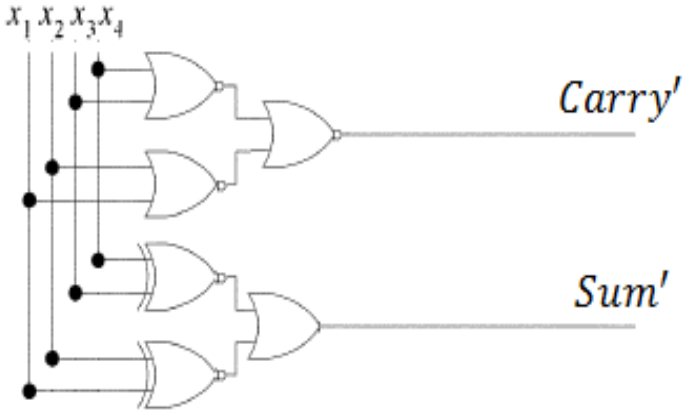


Figure 2.4: Implementation of gate level design2

$$Sum' = (\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$
$$Carry' = \overline{(x1x2 + \overline{x3x4})}$$

Table demonstrates reality table of the second inexact configuration for a 4-2 compressor this Table additionally demonstrates the distinction between the accurate decimal estimation of the option of the inputs and the decimal estimation of the yields created by the rough compressor. For instance when all inputs are1, the decimal estimation of expansion of the inputs is4.However, the surmised compressor creates a 1 for the carry and sum. The decimal estimation of the yields for this situation is 3; Table demonstrates that distinction is - 1.

Table 3: Truth table of second proposed 4-2 compressor

X_4	X_3	X_2	X_1	carry'	sum'	difference
0	0	0	0	0	1	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	-1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	1	-1
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	-1

This outline has in this way 4 incorrect outcomes out of 16 outcomes, so its mistake rate is currently decreased to 25%. This is an extremely positive component, since it demonstrates that on a probabilistic premise, the imprecision of the proposed outline is littler than the other accessible schemes.

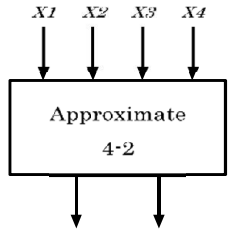


Figure 2.5: Approximate design2 (4-2 compressor)

III. MULTIPLICATION

In this area, the effect of utilizing the proposed compressors for multiplication is researched. A quick (correct) multiplier is normally made out of three sections (or modules) [4].

- Partial product generation.
- A Carry Save Adder (CSA) tree to lessen the fractional items' grid to an expansion of just two operands
- A Carry Propagation Adder (CPA) for the last calculation of the paired result. In the configuration of a multiplier, the second module assumes a critical part as far as deferral, force utilization and circuit intricacy. Compressors have been broadly utilized [11, 1] to accelerate the CSA tree and diminishing its energy dissemination, so to accomplish quick and low-control operation. The utilization of inexact compressors in the CSA tree of a multiplier results in an estimated multiplier.

An 8×8 unsigned Dadda tree multiplier is considered to evaluate the effect of utilizing the proposed compressors as a part of rough multipliers. The proposed multiplier uses in the main part AND doors to create every single halfway item. In the second part, the estimated compressors proposed in the past segment are used in the CSA tree to decrease the fractional items. The last part is an accurate CPA to register the last paired result. Figure (a) demonstrates the decrease hardware of a definite multiplier for n=8. In this figure, the lessening part utilizes half-adders, full-adders and 4-2 compressors; every incomplete item bit is spoken to by a speck.

In the main stage, 2 half-adders, 2 full-adders and 8 compressors are used to decrease the incomplete items into at most four lines. In the second or last stage, 1 half-viper, 1 full-snake and 10 compressors are utilized to figure the two last lines of halfway items. In this way, two phases of decrease and 3 half-adders, 3 full-adders and 18 compressors are required in the lessening hardware of a 8×8 Dadda multiplier

In this paper, four cases are considered for outlining an estimated multiplier.

In the principal case (Multiplier 1), Design 1 is utilized for every one of the 4-2 compressors in Figure

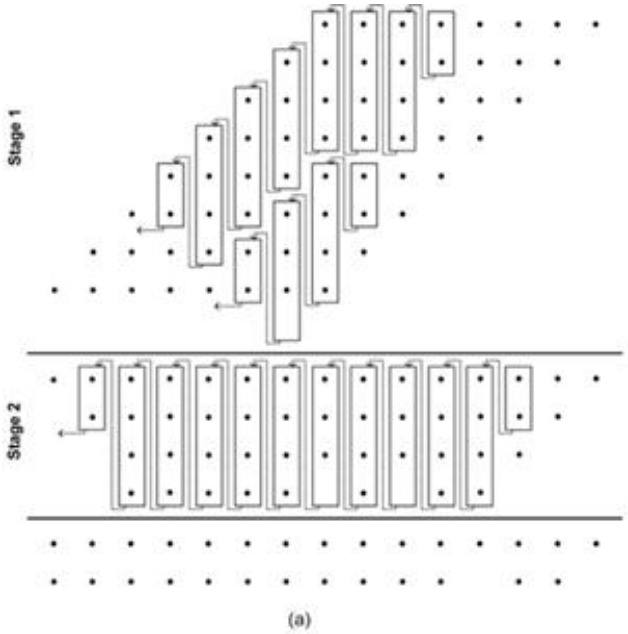


Figure 3.1: Reduction circuitary of an 8x8 Dadda multiplier using design1 compressors

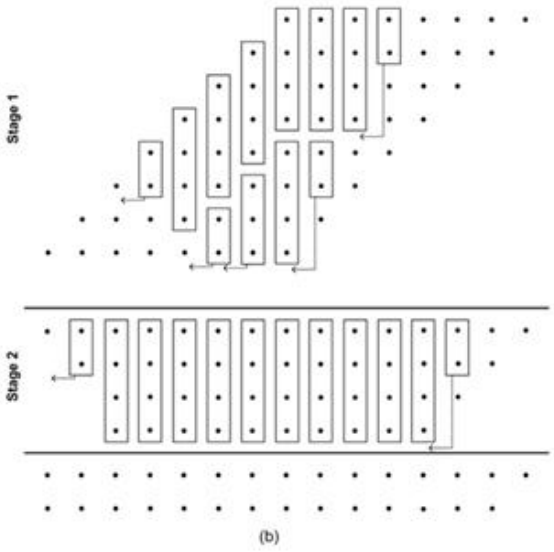


Figure 3.2: Reduction circuitary of an 8x8 Dadda multiplier Using design2 compressors.

• In the second case (Multiplier 2), Design 2 is utilized for the4-2 compressors. Since Design 2 does not have cin and cout, the lessening hardware of this multiplier requires a lower number of compressors (Figure (b)). Multiplier 2 utilizes 6 half-adders, 1 full-Adder and 17 compressors

• In the third case (Multiplier 3), Design 1 is utilized for the compressors as a part of then-1 minimum significant segment. The other n most noteworthy segments in the lessening hardware use careful 4-2 compressors. In the fourth case (Multiplier 4), Design 2 and precise 4-2 compressors are utilized as a part of them=1 slightest huge sections and afterward most critical segments in the decrease hardware individually.

IV. MODEL RESULTS:

A. Approximate Compressors

The two inexact compressors of this paper and the best low-control definite compressor of [4] (actualized by utilizing XOR-XNOR gates) are mimicked at the designs; a fan-out of is used in all re-enactments. The recreation aftereffects of the delay, power utilization LUT and slices.

Design 1: delay=26.195ns; LUT=107; Slices=56;

Design 2: delay=23.419ns; LUT=104; Slices=59;

The two proposed estimated designs accomplish noteworthy change as far as force consumption; on normal at various component sizes, the force utilization of Design 1 is 57% not exactly the precise compressor, while Design 2 has a force utilization that is 60% not exactly the careful configuration of [4].Table III thinks about these outlines regarding number of transistors, as a measure of circuit complexity. The definite compressor [4] utilizes 10 transistors to actualize each XOR* gates, 6 transistors to execute the XOR door and 8 transistors to actualize each MUX gate [4]; accordingly, the accurate compressor uses 52 transistors. A half change in circuit multifaceted nature is proficient by Design 2, as reflected by the lower number of transistors. This is normal in light of the fact that the second inexact configuration has no cin and cout with just 4 inputs and 2 outputs (the definite compressor has 5 inputs and 3 outputs).

B. Rough Multipliers:

The four proposed rough multipliers are recreated for n=8. The delay, power utilization and number of transistors are explored for these rough outlines and the accurate multiplier. A correlation of the mistake separation (as measure of unwavering quality [13]) of the proposed multipliers with other rough multipliers is additionally sought after.

Delay:

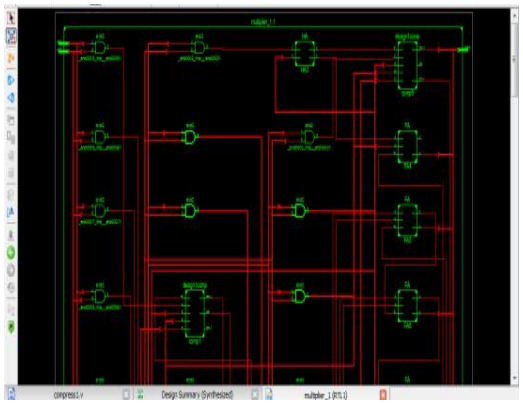
The delay of the decrease hardware (second module) of a Dadda multiplier is subject to the quantity of diminishment stages and the deferral of every stage. In Multipliers 1 and 2, the surmised compressors are utilized as a part of all sections; in this way, the delay of the stages is equivalent to the delay of the approximate compressors. However, in Multipliers 3 and 4, the delay of the stages is equivalent to the delay of the precise compressors. Along these lines, the utilization of these rough compressors in the n/2 LSBs cause no change regarding delay contrasted with a definite multiplier.

Power Consumption:

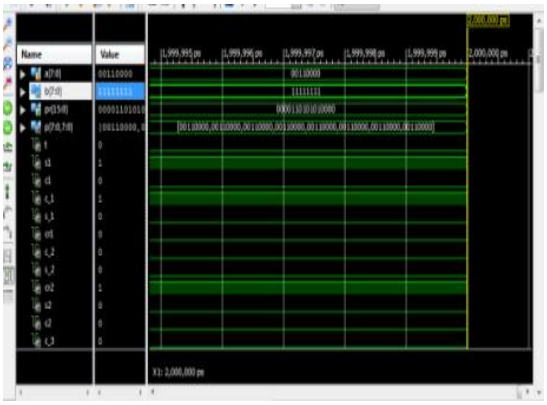
The force utilization of every multiplier is controlled by the number and kind of compressors utilized. Multipliers 1 and 2 utilize just approximate compressors so they have power utilization lower than Multipliers 3 and 4.

4.1. DESIGN 1 (SIMULATION AND SYNTHESIS REPORTS)

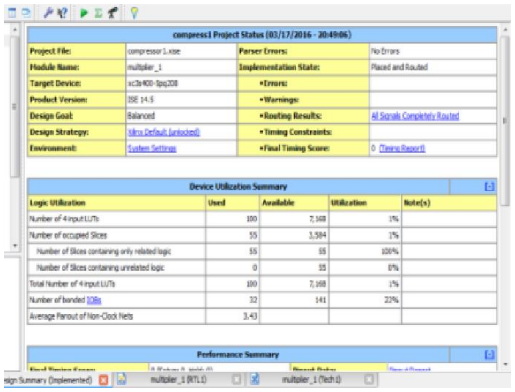
Schematic RTL:



Result:



Combination report:



compress1 Project Status (03/17/2016 - 20:49:06)

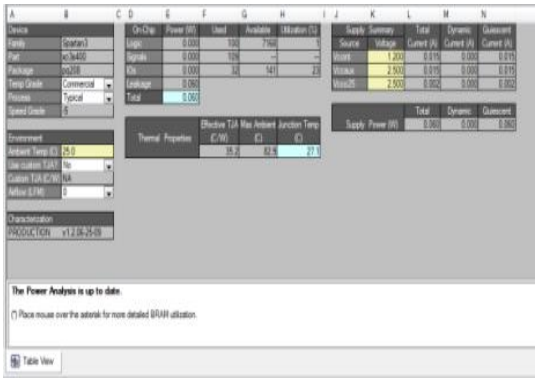
Project File:	compressor1.xise	Parser Errors:	No Errors
Module Name:	multiplier_1	Implementation State:	Placed and Routed
Target Device:	xc3s400-5pq208	•Errors:	
Product Version:	ISE 14.5	•Warnings:	
Design Goal:	Balanced	•Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	100	7,168	1%	
Number of occupied Slices	55	3,584	1%	
Number of Slices containing only related logic	55	55	100%	
Number of Slices containing unrelated logic	0	55	0%	
Total Number of 4 input LUTs	100	7,168	1%	
Number of bonded IOBs	32	141	22%	
Average Fanout of Non-Clock Nets	3.43			

Performance Summary

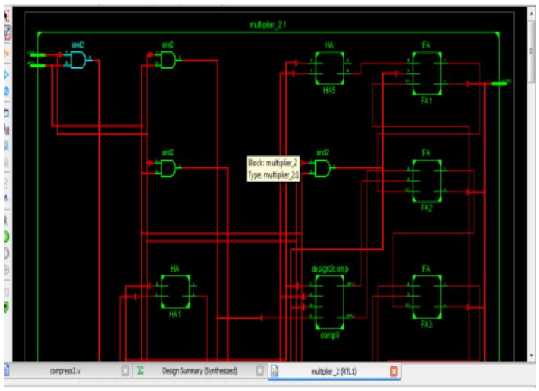
Port report:



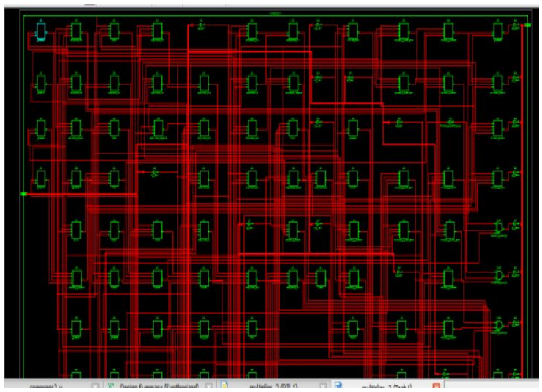
The Power Analysis is up to date.

4.2. DESIGN 2(SIMULATIONS AND SYNTHESIS REPORTS)

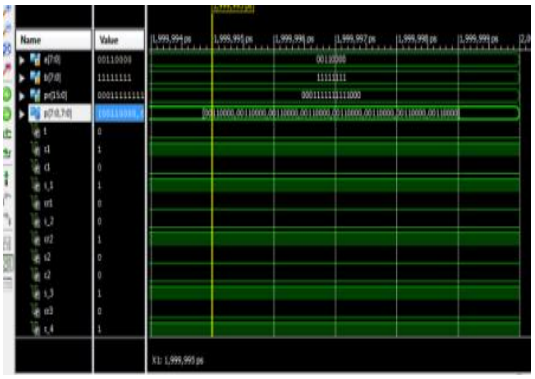
Schematic RTL:



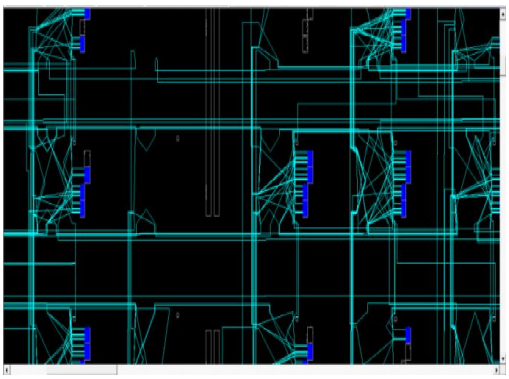
schematic Technology:



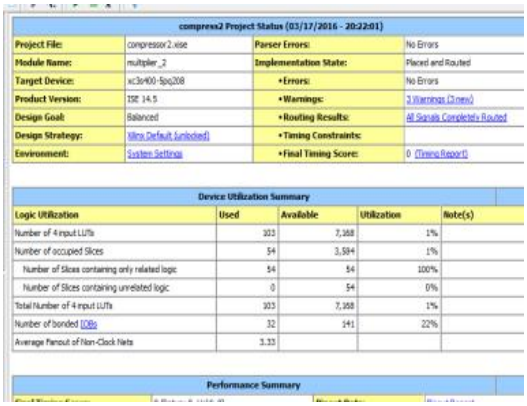
Result for Simulation:



Design of View route



combination report:

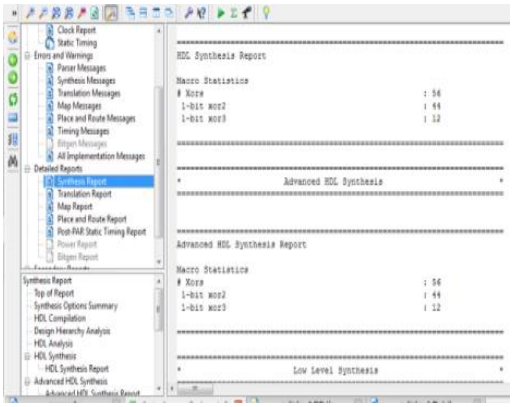


compressx2 Project Status (03/17/2016 - 20:22:01)			
Project File:	compressor2.xise	**Parser Errors:**	No Errors
Module Name:	multiplier_2	**Implementation State:**	Placed and Routed
Target Device:	xc3s400-5pq208	**•Errors:**	No Errors
Product Version:	ISE 14.5	**•Warnings:**	3 Warnings (3 new)
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

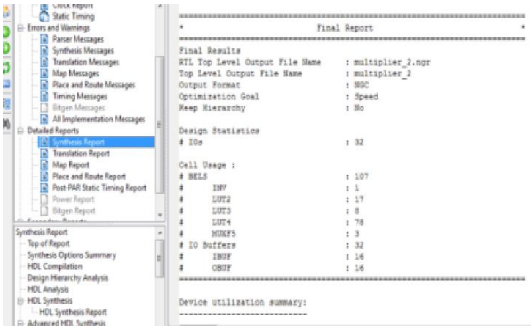
Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	103	7,168	1%	
Number of occupied Slices	54	3,584	1%	
Number of Slices containing only related logic	54	54	100%	
Number of Slices containing unrelated logic	0	54	0%	
Total Number of 4 input LUTs	103	7,168	1%	
Number of bonded IOBs	32	141	22%	
Average Fanout of Non-Clock Nets	3.33			

Performance Summary

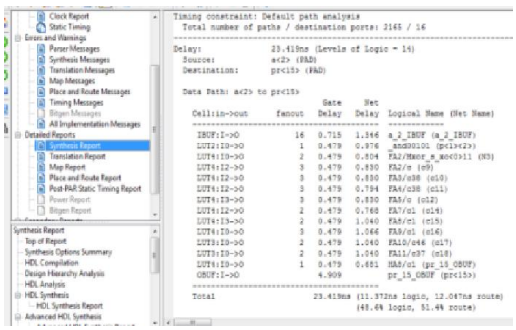
Port report:



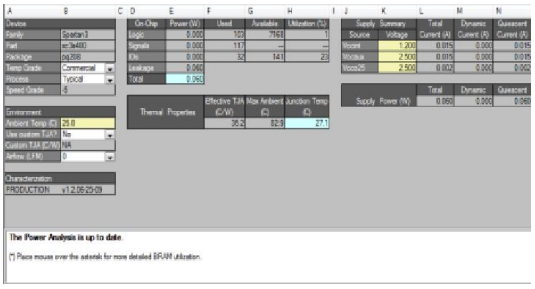
Lut slices:

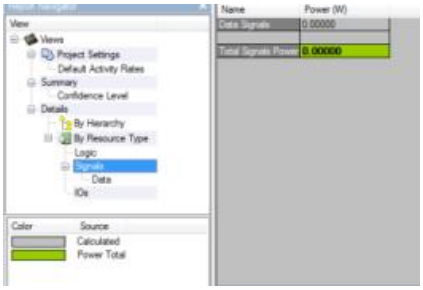


Timing delay



Power report:





Total power:

Name	Power (W)	I/O Standard	Signal Rate	% High	Clock (MHz)	Clock Name	Input Pins	Output Pins	Bidir Pins
IOs									
a (8)	0.00000	LVCMOS25	0.0	50.0	Async	Async	8	0	0
b (8)	0.00000	LVCMOS25	0.0	50.0	Async	Async	8	0	0
pr (16)	0.00000	LVCMOS25_12_SLOW	0.0	36.6	Async	Async	0	16	0
Total	0.00000					Count	16	16	0

Name	Power (W)	I/O Standard	Signal Rate	% High	Clock (MHz)	Clock Name	Input Pins	Output Pins	Bidir Pins
IOs									
a (8)	0.00022	LVCMOS25	30.0	50.0	Async	Async	8	0	0
b (8)	0.00022	LVCMOS25	30.0	50.0	Async	Async	8	0	0
pr (16)	0.02648	LVCMOS25_12_SLOW	20.0	50.0	Async	Async	0	16	0
Total	0.02692					Count	16	16	0

Implementation output for FPGA:

V. CONCLUSION

Inaccurate figuring is a rising worldview for calculation at Nanoscale. Computerized arithmetic offers huge operational favourable circumstances for inaccurate computing; a broad writing exists on inexact adders. In any case, this paper has at first centered on compression as utilized as a part of a multiplier. This paper has exhibited the usage of surmised 4-2 compressors in dada multipliers. These approximate results displayed in this composition.

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