DESIGN AND CONTROL OF HYBRID CASCADED MULTILEVEL CONVERTER FOR HVDC APPLICATIONS

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Abstract- Hybrid multilevel converters are contemplated in an attempt to optimize the performance of voltage source converters in terms of magnitude of semiconductor losses and converter footprint, and to achieve additional features such as dc short circuit proof, which is essential for a high integrity multi-terminal HVDC grid. Therefore, this paper considers an emerging hybrid cascaded converter that offers the dc side short circuit proof feature at reduced loss and footprint compared to the existing multilevel and other hybrid converters. Its operating principle, modulation and capacitor voltage balancing strategies are described in detail. Furthermore, hybrid converter scalability to high voltage applications is investigated. The validity of the modulation and capacitor voltage strategy presented are confirmed using simulation and experimentation. The hybrid cascaded converter is extendable to a large number of cells, making it applicable to high voltage applications, and operation is independent of modulation index and power factor. On these ground, the converter is expected to be applicable for both real and reactive power applications.

Key words : **DC fault reverse blocking capability; half and full-bridge modular multilevel converters; hybrid multilevel converters; and voltage source converter based high-voltage direct current transmission systems.**

1 INTRODUCTION

The recent increased in use of voltage source converters in medium and high voltage applications has motivated academics and industrial researchers to develop alternative converter topologies that address some of the limitations of the modular converter regarding level of semiconductor losses and footprint[1-17].

Currently the modular multilevel converter (MMC) is widely adopted by many HVDC manufacturers for high dc and flexible ac transmission system applications [7, 18-28]. However, the flow of three current components in the converter arms that are associated with the converter's ac and dc power exchanges, plus the circulating currents between converter arms, represent a major concern

as these increase semiconductor losses significantly [11, 16, 19-22, 25, 29-38]. Furthermore, the large number of sizeable cell capacitors in the modular converter arms is seen as a major barrier, hampering its adoption in offshore applications where platform costs represents a significant portion of the overall capital cost. These concerns are exacerbated by vulnerability to dc side faults, as the half-bridge modular converters are unable to block an ac grid contribution so as to suppress dc link faults [10, 39, 40]. This paper describes the operational principle, modulation and capacitor voltage balancing of the hybrid converter presented in [46], which is called throughout this paper as hybrid cascaded converter with dc side H-bridge cell.. The scalability of the hybrid cascaded converter to medium and high applications is investigated. The discussions show that the hybrid multilevel converter being investigated in this paper is promising in wide range of applications as well as its scalability to a large number of cells, with minor modifications needed to the control and modulation of the established modular converter.

2 LITERATURE REVIEW

[1] New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources 2012

A cascaded multilevel inverter made up of from series connected single full bridge inverter, each with their own isolated dc bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources, which may be obtained from solar cells, fuel cells, batteries, ultra capacitors, etc. This type of converter does not need any transformer or clamping diodes or flying capacitors [16].Each level can generate five different voltage outputs +2Vdc, +vdc, 0 ,–2Vdc and –vdc by connecting the dc sources to the ac output side by different combinations of the four switches. The output voltage of an M-level inverter is the sum of all the individual inverter outputs. Each of the H-Bridge's active devices switches only at the fundamental frequency, and each H-bridge unit generates a quasi- square waveform by phase-shifting its positive and negative phase legs switching timings. Further, each switching device always conducts for 180° (or half cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device [17].This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency.

A single-phase multilevel cascade Inverter topology is essentially composed of single identical phase legs of the series-chain of H-bridge inverter, which can possibly generate different output voltage waveforms and offers the potential for ac system phase-balancing. The converter topology is based on the series connection of single-phase inverters with separate dc sources the resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a five level cascaded inverter each single-phase full-bridge inverter generates five voltages at the output:+Vdc, + 2vdc, 0,-Vdc and -2vdc.

[2] Improved Active Power Filter Performance for Renewable Power Generation Systems

Renewable generation affects power quality due to its nonlinearity, since solar generation plants and wind power generators must be connected to the grid through high power static PWM converters [1]. The non-uniform nature of power generation directly affects voltage regulation and creates voltage distortion in power systems. This new scenario in power distribution systems will require more sophisticated compensation techniques. PI controllers must be designed based on the equivalent linear model, while predictive controllers use the non-linear model, which is closer to real operating conditions. An accurate model obtained using predictive controllers improves the performance of the active power filter, especially during transient operating conditions, because it can quickly follow the current-reference signal while maintaining a constant dc-voltage.

Four-Leg Converter Model

Both types of power generation use AC/AC and DC/AC static PWM converters

for voltage conversion and battery banks for long-term energy storage. These converters perform maximum power point tracking to extract the maximum energy possible from wind and sun. The electrical energy consumption behavior is random and unpredictable.
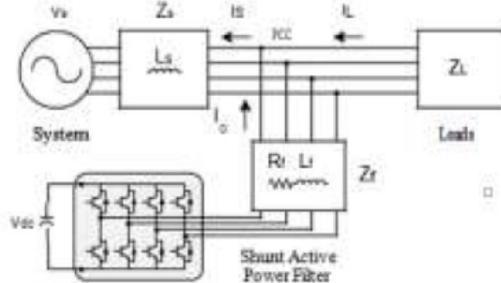
Figure 2.1: Three-phase equivalent circuit of the proposed shunt active power filter.

The block diagram of the proposed digital predictive current control scheme is shown in Fig. 1.This control scheme is basically an optimization algorithm and therefore it has to be implemented in a microprocessor. Consequently, the analysis has to be developed using discrete mathematics in order to consider additional restrictions such as time delays and approximations. The main characteristic of predictive control is the use of the system model to predict the future behavior of the variables to be controlled.

[3] Cascaded multilevel converter based transmission STATCOM 2012

This research and development work deals with the design methodology for Cascaded Multilevel Converter (CMC) based Transmission STATCOM (TSTATCOM) and development of a ±12MVAR, 12kV line-to-line wye-connected, 11-level CMC. This CMC module constitutes the basic building block of TSTATCOM systems. Sizing of the CMC module, number of H-Bridges in each phase of the CMC, AC voltage rating of the CMC, the number of paralleled CMC modules in the T-STATCOM system, optimum value of series filter reactors and determination of busbar in the power grid to which the T-STATCOM system is going to be connected are also discussed in the thesis in view of IEEE Std.519-1992, current status of HV IGBT technology and the required reactive power variation range for the T-STATCOM application. In the field prototype of the CMC module, the AC voltages are approximated to sinusoidal waves by Selective Harmonic Elimination Method (SHEM) and by the use of an optimized series input filter reactor.

Design works for HB and the CMC are based on MATLAB and PSCAD simulations. The laboratory and field performance of the HB circuit and CMC module is found to be satisfactory and quite consistent with the theoretical results and design objectives. In addition to these, 154 kV, ±50MVAr T-STATCOM prototype has been designed, implemented and installed at Sincan Transformer Substation-Ankara primarily for the purposes of reactive power compensation and terminal voltage regulation. The T-STATCOM prototype is composed of five parallel operated CMC modules developed within the scope of this PhD thesis research work.

3 EXISTING SYSTEM

3.1 Design of CMC Module

In this work, a 3-phase, Y-connected, 11-level (n=5), ±12MVAr H-Bridge based Cascaded Multilevel Converter (CMC) module shown in Figure 3.1 is designed and implemented. AC voltage of the CMC is chosen to be Vc = 12 V line-to- line and its constant DC link voltage is Vdc=9500V. In each phase of the CMC, five HB circuits are connected in series and the DC link voltage of the designed HB is Vd=1900Volts mean. HB units used in each phase of CMC module have been placed on the shelves which are built up of a specially designed Glass-fiber Reinforced Polyester (GRP) with 3x5 matrix structure as shown in Figure 3.1.

In this section, the design considerations for CMC module and the HB circuit with the selection of its major components like power semiconductors, laminated busbars, and DC link

capacitors have been presented. Moreover, the control system with its structure and its major functions for a CMC module is also given in this section.
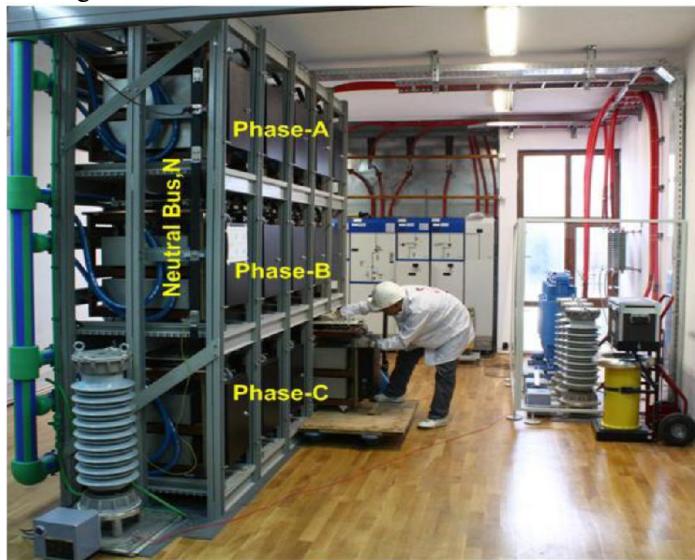
Figure 3.1: Designed and implemented 3-phase, 12kV, ±12 MVAr, Y-connected 11-level CMC module

3.1.1 Design of the H-Bridge (HB) Circuit

H-Bridge circuits are the basic units for the power stages of CMC modules. In fact, **n** number of HBs can be connected in series for each phase of CMC to reach the desired AC voltage at which CMC is implemented. This gives a modularized circuit layout and packaging for CMC due to the usage of the same structure for each level.

3.1.2 The structure and operation of HB Circuits

Figure 3.2 shows the single line diagram of an H-Bridge (HB) circuit with its typical output voltage. In an HB circuit, as power semiconductors, there are four conventional wire-bond HV IGBT modules in which antiparallel diodes are used with IGBT parts in the same packages. The operation states of the HB and diode parts of the HV IGBT modules are dependent upon the direction of the current. As an example, if polarity of the current flowing through the HB circuit is taken as positive, +Vd is obtained as output voltage of HB by the operation of diodes, D1-D3. The same output voltage is also seen by the operation of S1-S3 when current flowing out of the HB. Zero voltage level exits when current is bypassed through the DC link voltages.
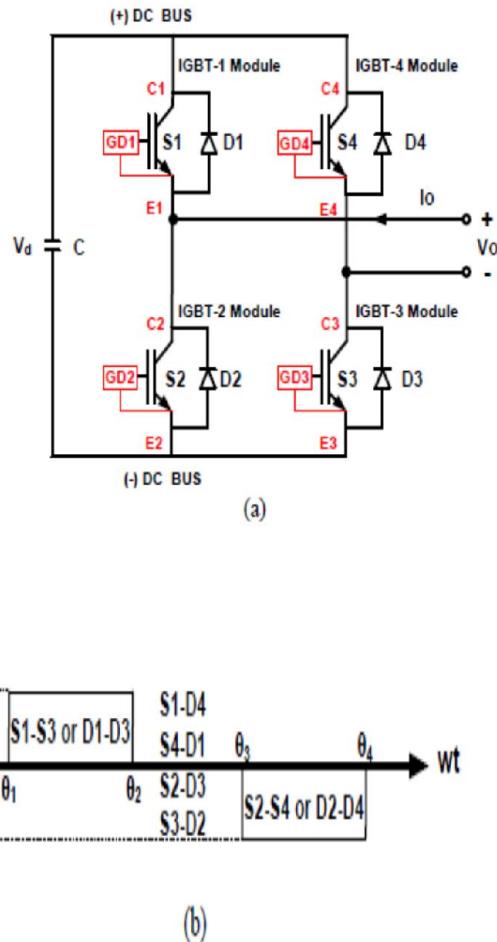
Figure 3.2: Single line diagram of (a) the HB circuit and (b) it typical output voltage

The operation mode of any HB in the CMC at any time and duration of this mode are determined by modulation index value, M and DC link equalization method (MSS with Δts = 400μs). Furthermore, M dictates how many of five HBs are to be operated in by-pass mode at any time.
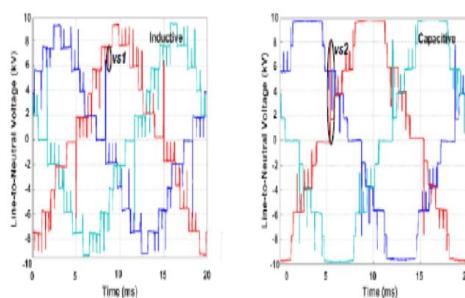
Figure 3.3: Voltage spikes superimposed on the line-to-neutral CMC voltages with MSS method

On the other hand, which HBs are to be operated in charging or discharging mode, is dictated by the equalization algorithm of DC link capacitor voltages. For each step of the 11-level line-to-neutral voltage waveform, operation modes for all HBs and the number of HBs in each mode are also

marked in Figure 3.3 and Figure 3.5. In order to avoid complexity in the explanations, the theoretical line-to-neutral voltage waveform prepared for Conventional Selective Swapping (CSS) method.

3.1.3 Programmable Logic Controller (PLC)

The Programmable Logic Controller (PLC) achieves control actions according to the signals received from the DSP Board and external sub-systems via digital/analog I/Os and data acquisition and state monitoring actions received from the same system elements via serial communication channels. The major operational features of the PLC are as described below:

a. The PLC carries out data acquisition, state monitoring and fault diagnosis actions according to the signals taken from the DSP Board and external subsystems.

b. The operation state of the T-STATCOM system (on/off operation of circuit breakers and the load-break switch) is commanded by the PLC according not only to the protection signals received from the de-ionized water cooling system but also to on/off or protective signals received from other system elements.

The de-ionized water cooling system is therefore turned on by the PLC before re-closing action of the main CB to provide cooling service for power semiconductors. The classified and unclassified fault/failure data are also sent to the industrial computer for monitoring purpose.

3.2 Field Performance of HB

In order to avoid any undefined operational state for H-Bridge (HB) circuits, the gates of all IGBT modules in each HB receive either +15V DC or -15V DC control signal. When -15V DC is applied, the IGBT part turns off but its anti-parallel diode may carry negative module current. However, when +15V DC is applied, the IGBT part not necessarily triggers into conduction but its anti-parallel diode may carry the negative module current.

Among FACTS devices, the shunt controllers have shown feasibility in terms of in a wide range of problem-solving abilities from transmission to distribution levels. For decades, it has been realized that by manipulating the compensated reactive power, the transmittable active power through the interconnected networks can be increased without installing new transmission lines and the voltage profile of the buses can also be controlled easily by the shunt controllers.

4 PROPOSED SYSTEM

4.1 Hybrid Multilevel Operating Principle

Fig. 4.1(a) shows a single-phase hybrid cascaded converter with two dc side H-bridge cells. When the capacitor voltage across each dc side H-bridge cell is regulated at $\frac{1}{2}V_{dc}$, five output voltage va, levels (V_{dc}, $\frac{1}{2}V_{dc}$, 0, $-\frac{1}{2}V_{dc}$, $-V_{dc}$) can be generated between terminals a1 and a2. The switch states that generate these five voltage levels are summarized in Table 1.

The switch states of the H-bridge cells that can be utilised to generate voltage levels V_{dc} and $\frac{1}{2}V_{dc}$ are the same as those for generation of voltage levels $-V_{dc}$ and $-\frac{1}{2}V_{dc}$. The converter output voltage is synthesized according to:

$$v_a = [V_{dc} - V_{HB}(t)](S_1 - S_3)$$

where *Vdc* is dc link voltage, *N* is the number of dc side H-bridge cells, *Vcj* is the cell capacitor voltage of the *jth* cell, and S1 and S3 represent the switch states of the two upper switches of the main bridge connected to the load, see Fig. 4.1.

In this manner, the voltage across dc side cascaded bridge cells which represents the term in equation (1), can be expressed by:

$$V_{HB}(t) = V_{dc}[1 - m|\sin \omega t|]$$

This means the dc voltage applied across the dc input of the main H-bridge cell is:

$$V_m(t) = V_{dc} - V_{dc}[1 - m|\sin \omega t|] = mV_{dc}|\sin \omega t|$$

On this basis converter, the output voltage can be expressed.
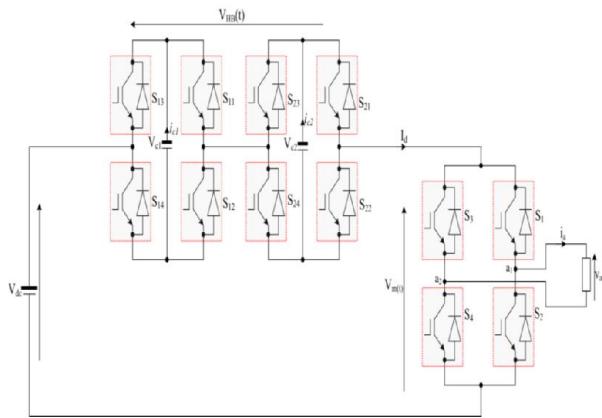
(a) Illustrative two-cell version of the hybrid cascaded converter with dc side H-bridge cells
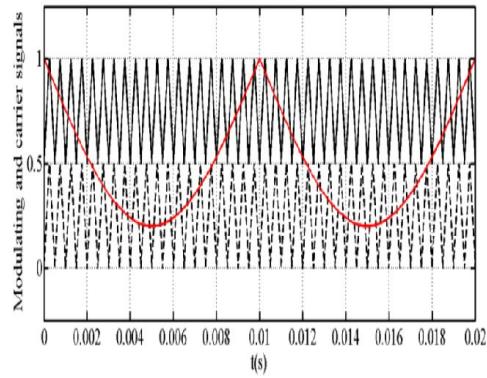
(b) Phase dispossition carriers and H-bridge cells modulation signal
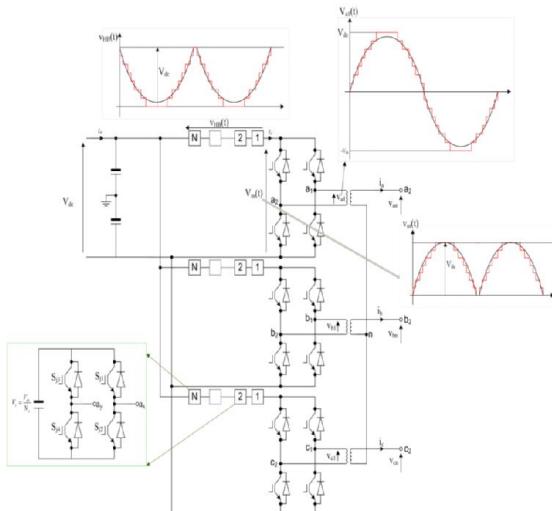
(c) Generic version of the hybrid cascaded converter with dc side H-bridge cells
Figure 4.1: Hybrid cascaded multilevel converter with dc side H-bridge cells

In order words, the main bridge operates every negative half cycle to flip the input dc rectified voltage to produce the negative half of the output voltage. A phase disposition (PD) carrier

arrangement is adopted because it minimizes the number of switching transitions per carrier period, compared to the phase shifted (PS) carriers for the same carrier frequency and produces centred aligned pulses (improved harmonic performance at reduced switching frequency per device). Capacitor voltage balancing is achieved by rotating the cell capacitor every sampling period depending on the polarity of the limb current Id, and voltage magnitude of each individual cell. For this two-cell version of the hybrid cascaded converter in Fig. 4.1(a), assume current direction shown is the positive, the cell capacitor with a minimum voltage is selected to charge when $Id>0$, while that with a maximum voltage is selected to discharge, and the opposite is true when $Id<0$. But the exact number of cell capacitors to be selected in each sampling period is determined by the voltage level to be synthesized, according to modulation function of the H-bridge cells .

Table 1: Summary of switch states of the hybrid converter with two dc side H-bridge cells and their influence on the cell capacitor state of charge ($\uparrow$, $\downarrow$ and $\rightarrow$ indicate charging, discharging and unchanged respectively)

Voltage levels	Main bridge switch states	H-bridge cells switch states	$I_d>0$	$I_d<0$
V_{dc}	$S_1=1$ and $S_2=0$	i. $S_{11}=S_{12}=1$ and $S_{21}=S_{22}=1$	$C_1\rightarrow$ and $C_2\rightarrow$	$C_1\rightarrow$ and $C_2\rightarrow$
		ii. $S_{11}=1$, $S_{12}=0$ and $S_{21}=0$, $S_{22}=1$	$C_1\downarrow$ and $C_2\uparrow$	$C_1\uparrow$ and $C_2\downarrow$
		iii. $S_{11}=0$, $S_{12}=1$ and $S_{21}=1$, $S_{22}=0$	$C_1\uparrow$ and $C_2\downarrow$	$C_1\downarrow$ and $C_2\uparrow$
$\frac{1}{2}V_{dc}$	$S_1=1$ and $S_2=0$	iv. $S_{11}=0$, $S_{12}=1$ and $S_{21}=S_{22}=1$	$C_1\uparrow$ and $C_2\rightarrow$	$C_1\downarrow$ and $C_2\rightarrow$
		v. $S_{11}=S_{12}=1$ and $S_{21}=0$, $S_{22}=1$	$C_1\rightarrow$ and $C_2\uparrow$	$C_1\rightarrow$ and $C_2\downarrow$
0	$S_1=1$ and $S_2=0$ or $S_1=0$ and $S_2=1$	vi. $S_{11}=0$, $S_{12}=1$ and $S_{21}=0$, $S_{22}=1$	$C_1\uparrow$ and $C_2\uparrow$	$C_1\downarrow$ and $C_2\downarrow$
$-\frac{1}{2}V_{dc}$	$S_1=0$ and $S_2=1$	vii. $S_{11}=0$, $S_{12}=1$ and $S_{21}=S_{22}=1$	$C_1\uparrow$ and $C_2\rightarrow$	$C_1\downarrow$ and $C_2\rightarrow$
		viii. $S_{11}=S_{12}=1$ and $S_{21}=0$, $S_{22}=1$	$C_1\rightarrow$ and $C_2\uparrow$	$C_1\rightarrow$ and $C_2\downarrow$
$-V_{dc}$	$S_1=0$ and $S_2=1$	ix. $S_{11}=S_{12}=1$ and $S_{21}=S_{22}=1$	$C_1\rightarrow$ and $C_2\rightarrow$	$C_1\rightarrow$ and $C_2\rightarrow$
		x. $S_{11}=1$, $S_{12}=0$ and $S_{21}=0$, $S_{22}=1$	$C_1\downarrow$ and $C_2\uparrow$	$C_1\uparrow$ and $C_2\downarrow$
		xi. $S_{11}=0$, $S_{12}=1$ and $S_{21}=1$, $S_{22}=0$	$C_1\uparrow$ and $C_2\downarrow$	$C_1\downarrow$ and $C_2\uparrow$

Table 1 summarises the number of cell capacitors to be selected at each voltage level, and the charging and discharging behaviour of each individual cell for a given limb current Id polarity. A voltage band of 10% of $\frac{1}{2}Vdc$ is imposed on the cell capacitor voltages to prevent extreme discharge or overcharge at voltage levels $\pm Vdc$.

4.2 Circuit Diagram
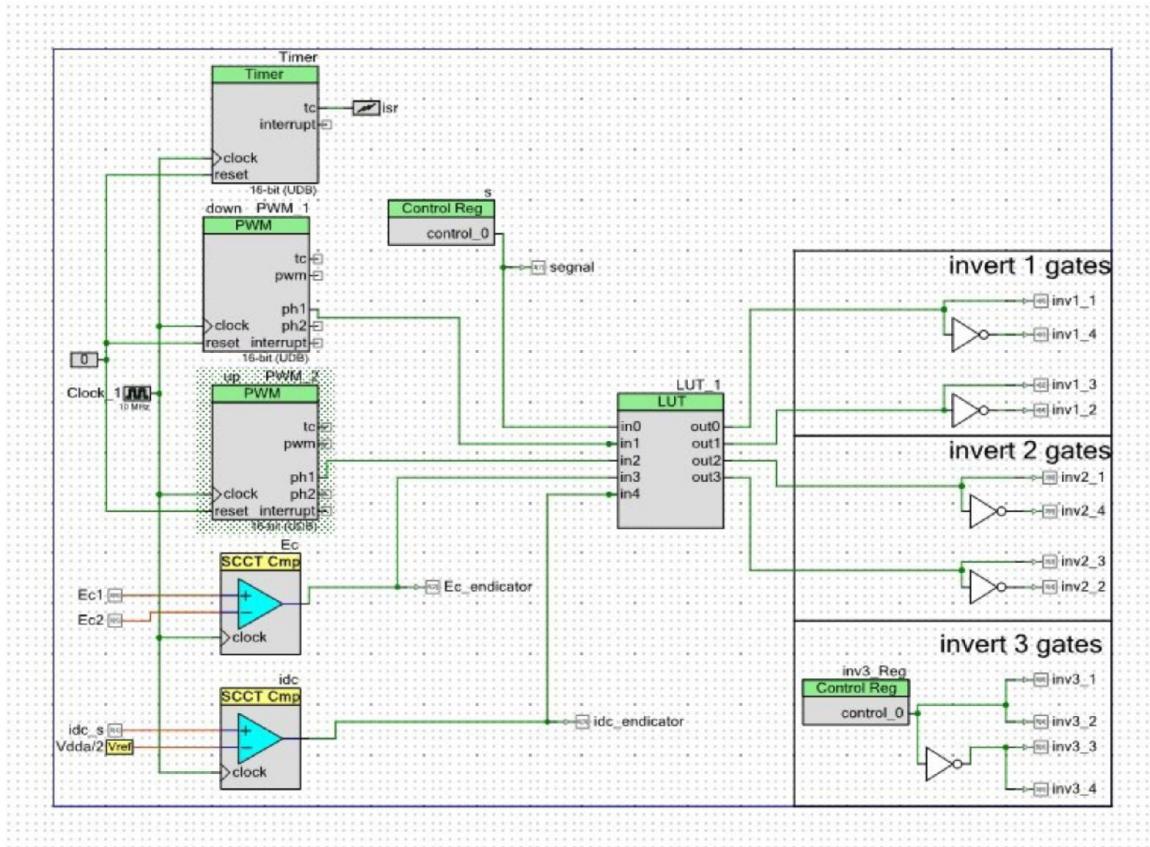
Figure 4.2: Circuit diagram of proposed method of multilevel cascade inverter

The circuit diagram of proposed method of multilevel cascade inverter as shown in Figure 4.2.The circuit diagram of operation mode with proposed method of single phase five level cascaded H-Bridge multilevel inverter is shown in figure 4.3. It consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four POWER MOSFET switches. The inverter produces output voltage in five levels: V_{dc}, $2V_{dc}$, 0,$-V_{dc}$ and $-2V_{dc}$.

The cascaded H-bridges multilevel inverter introduces the idea of using separate DC sources to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source V_{dc}. By cascading the AC outputs of each H- bridge inverter, AC voltage waveform is produced.

Fig. 4.1(c) shows the three-phase version of the generic hybrid cascaded multilevel converter with N dc side cascaded H-bridge cells per limb. When the number of H-bridge cells is sufficiently high, high frequency pulse width modulation can be replaced by amplitude (staircase) modulation as shown in Fig. 4.1(c).

Furthermore, it generates the same voltage levels per phase as the MMC but with half the number of cells. Moreover, the hybrid cascaded converter is inherently dc short-circuit proof, where this feature is activated by inhibiting the gating signals to the converter switches, as the H-bridge cell capacitors will oppose any current flow; thus there is no current in converter switches and no power exchange between the converter ac and dc sides. However, the issues related to short circuit proof feature is out of scope of this paper. With a lossless power conversion assumption in both the dc side cascaded H-bridge cells and main bridge power stages, the power balanced equation assumes the ac side active power equals the dc power.

4.3 Simulations

This section presents simulation results when a single-phase hybrid converter with two H-bridge cells per limb is operated from a 120V supply. The simulation parameters are: *Vdc*=120V, cell capacitance *C*=2.2mF, and the converter is controlled using SPWM with a 2kH carrier frequency.

To illustrate the suitability of the hybrid cascaded for applications that require the converter terminal voltage to be varied, such as in HVDC applications, the modulation index is reduced to 0.4, and the load is reduced to 40% to maintain the load current near constant. The waveforms in Fig. 4.3 show that the hybrid converter is able to operate at reduced modulation, while exchanging power with the ac at near unity power factor.

To demonstrate the hybrid cascaded multilevel converters reactive power capability, the load power factor is reduced to 0.37 lagging (*R*=4□ and *L*=31.8mH) when the modulation index is *m*=0.9. The system is able to operate successfully with voltage stresses across switching devices controlled since voltage balancing of the H-bridge cell capacitors is maintained..
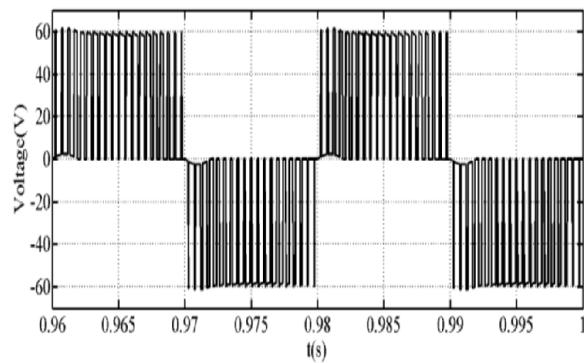
(a) Phase voltage '*va*'
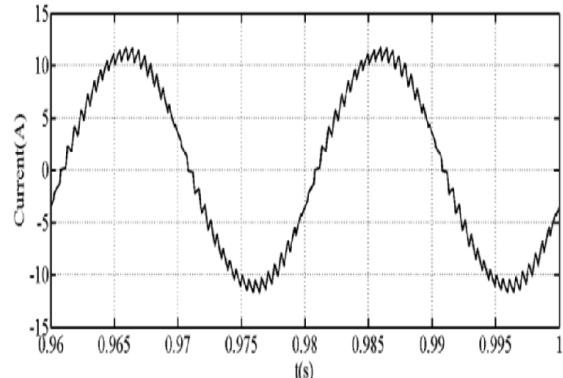
(b) Output phase current '*ia*'
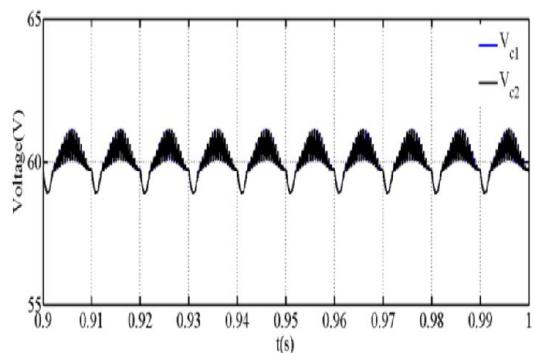
(c) Voltage across H-bridge cells

Figure 4.3: Waveforms illustrate hybrid cascaded converter operation at reduced modulation indices while delivering real power. (Vdc=120V, C=2.2mF, 2kHz switching frequency, and a load 4 and 4mH)

5 RESULT AND DISCUSSION

5.1 Scalability of The Hybrid Cascaded Multilevel Converter

The previous sections have confirmed the applicability of the hybrid cascaded converter in a wide range of applications. This section demonstrates its scalability to high-voltage applications where a large number of H-bridge cells per limb is necessary to permit the use of 3.3/4.5/6.5kV low-voltage rated switching devices. This demonstration uses a three-phase hybrid cascaded converter rated at 20MVA with a 20kV dc link, supplying a passive load of 20 Ω resistance and 15 Ω inductive reactance, through a 50Hz 13.8kV/24kV interfacing transformer, at 0.9 modulation index.

Simulation results are displayed with a relatively large number of cells per limb, hybrid cascaded converter produces high quality three-phase output voltage and currents with extremely low THD and *dv/dt*. Additionally, the voltage across dc side cascaded H-bridge cells and that across the dc input of the main bridge connected to interfacing transformer are in line with the theoretical waveforms depicted. The voltages across converter cell capacitors remain tightly balanced around the desired settle point of 1/11 * 20KV = 1.82Kv.

5.2 Screenshot
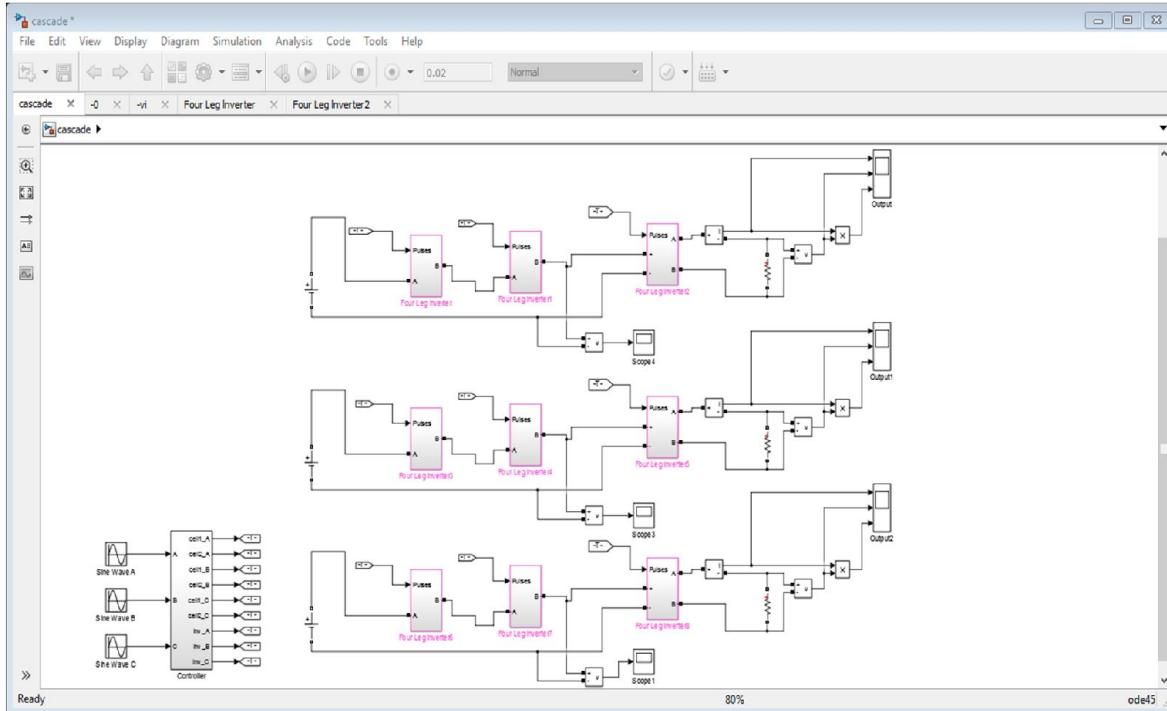
Figure 5.1: **Three phase Cascade**
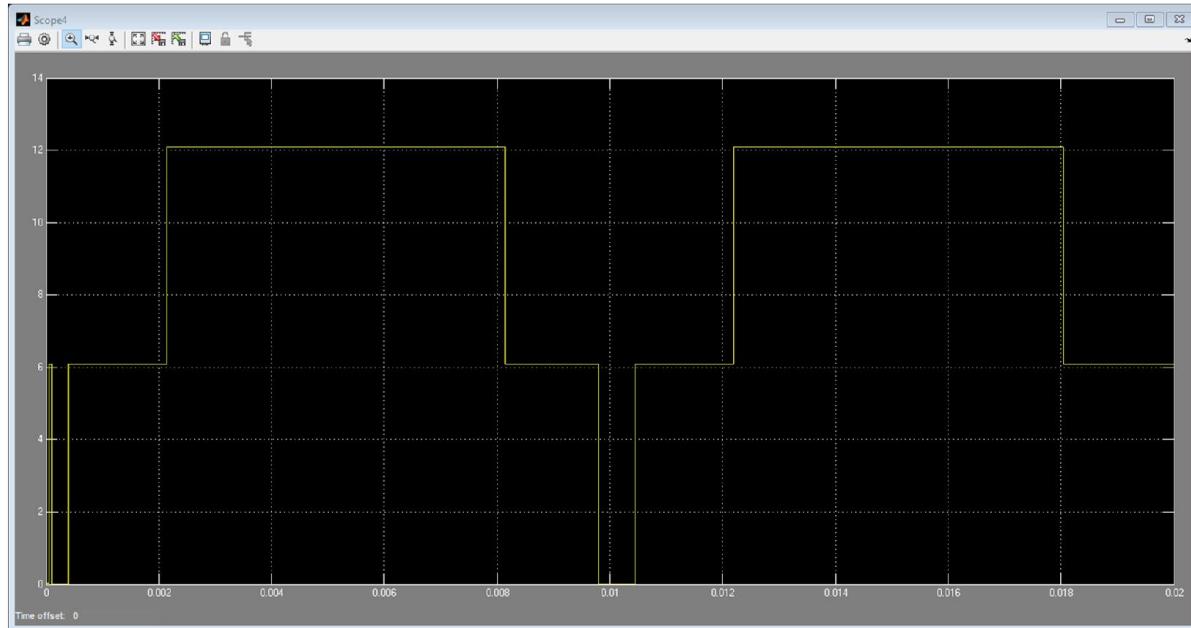
Figure 5.2: *Converter Output*
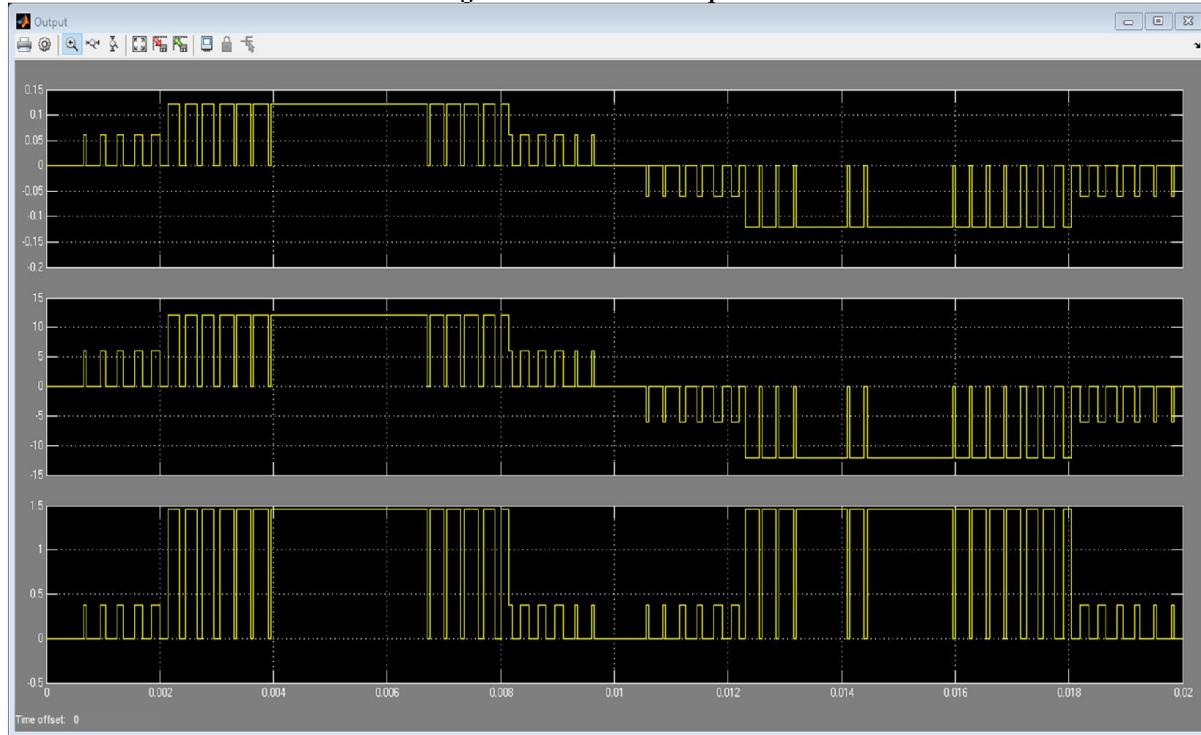
Figure 5.3: Inverter output

CONCLUSION

This paper presented the basic operational principle, modulation and capacitor voltage balancing of an emerging hybrid cascaded multilevel converter with dc side cascaded H-bridge cells. Simulations and experimentation were used to confirm the practicality of the hybrid cascaded converter, including its scalability to high-voltage applications. It has been shown that the hybrid cascaded converter with dc side cascaded H-bridge cells can operate over the entire P-Q envelope normally required for HVDC converters, without capacitor voltage balancing problems, and with voltage stresses on the converter switches evenly distributed. The main H-bridge converter that is connected to the load or interfacing transformer operates at fundamental frequency, while the effective switching frequency per device within the dc side cascaded H-bridge cells are low (in order of 150Hz or lower) when a large number of cells is used. Thus, low H-bridge switching loss is expected.

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